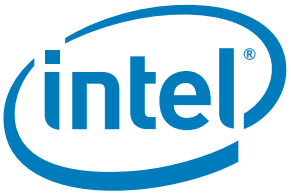


Second Generation Intel® Xeon® Scalable Processors

Thermal/Mechanical Specifications and Design Guide

July 2020

Reference Number: 616766-007US

Contents

Figures

Tables

Revision History

Document Number	Revision Number	Description	Revision Date
338747	001	• Initial release	April 2019
338747	002	• Updated Table 5-1, "Second Generation Intel® Xeon® Scalable Processors Non-MCP SKU Thermal Specifications" • Updated Table 5-4, "Second Generation Intel® Xeon® Scalable Processors - SP ISS Thermal Specifications"	June 2019
338747	003	• Updated Table 5-1, "Second Generation Intel® Xeon® Scalable Processors Non-MCP SKU Thermal Specifications" • Added Table 5-3, "Second Generation Intel® Xeon® Scalable Processors Refresh Non-MCP SKU Thermal Specifications" • Updated Table 5-4, "Second Generation Intel® Xeon® Scalable Processors - SP ISS Thermal Specifications"	June 2019
338747	004	• Updated Table 5-3, "Second Generation Intel® Xeon® Scalable Processors Refresh Non-MCP SKU Thermal Specifications"	August 2019
338747	005	• Updated SKU Intel® Xeon® Gold 5219W in Table 5-3, "Second Generation Intel® Xeon® Scalable Processors Refresh Non-MCP SKU Thermal Specifications"	September 2019
338747	006	• Added Section 5.1.2.1, "Designing for Turbo Performance: Intel® Turbo Boost Technology Testing" • Updated Table 11-1, "Second Generation Intel® Xeon® Scalable Processors Based Platform LGA3647-0 Socket Enabling Components"	November 2019
616766	007	• Updated Table 5-1, "Second Generation Intel® Xeon® Scalable Processors Non-MCP SKU Thermal Specifications" • Added Table 5-2, "Second Generation Intel® Xeon® Scalable Processors High Frequency Thermal Specifications" • Updated Table 5-3, "Second Generation Intel® Xeon® Scalable Processors Refresh Non-MCP SKU Thermal Specifications" • Updated Table 5-5, "Second Generation Intel® Xeon® Scalable Processors-SP_HT XCC Thermal Specs Update" • Reference Doc number changed from 338747 to 616766	July 2020

§

1 Introduction

This document provides specifications and guidelines for the design of thermal and mechanical solutions for the Second Generation Intel® Xeon® Scalable Processors.

1.1 Objective

This document explains and demonstrates the processor thermal and mechanical solution features and requirements. This document also provides an understanding of the processor thermal characteristics, and discusses guidelines for meeting the thermal requirements imposed on the entire life of the processor. As such, the purpose of this design guide is to describe the reference thermal solution and design parameters required for the Second Generation Intel® Xeon® Scalable Processors. The thermal/mechanical solutions described in this document are intended to aid component and system designers in developing and evaluating processor compatible solutions.

The components and information described in this document include:

- Thermal profiles and other processor specifications and recommendations
- Processor mechanical load limits
- Processor socket and board structural support
- Processor Heatsink Module (PHM) specifications and recommendations
- Heatsink specifications and recommendations

The goals of this document are:

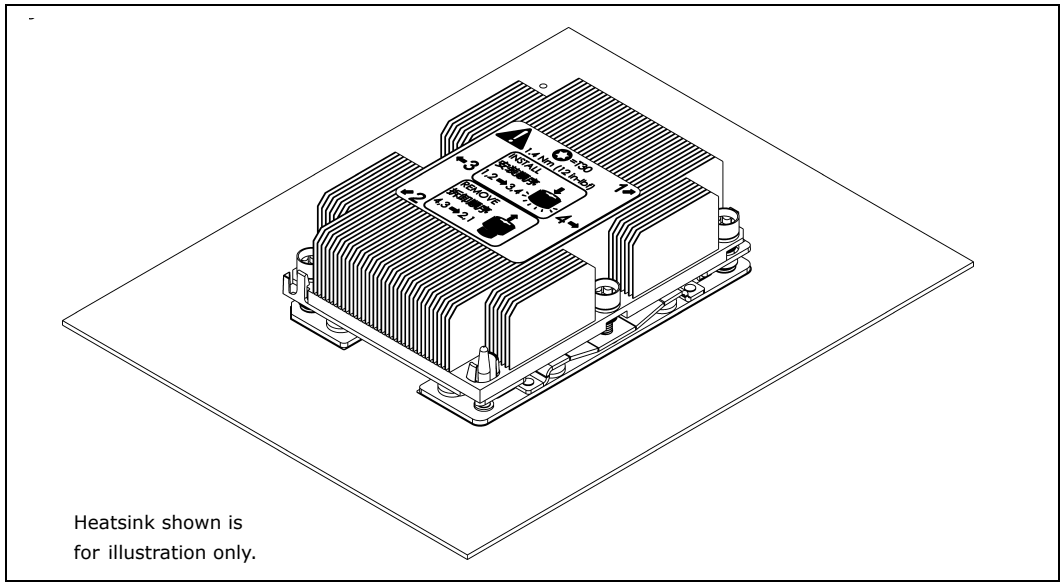
- To assist board and system thermal mechanical designers
- To assist designers and suppliers of processor heatsinks

1.2 Scope

The thermal/mechanical solutions described in this document pertain only to a solution(s) intended for use with the Second Generation Intel® Xeon® Scalable Processors in 1U, 2U, 4U form factor systems. This guide contains the mechanical and thermal requirements of the processor compatible cooling solution. Additional reference information is provided in the appendices of this document. The components described in this document include:

- The processor package
- The LGA3647-0 socket (socket P0)
- The Processor Heatsink Module (PHM) and the associated retention hardware
- Socket P0 retention mechanism

Figure 1-1. PHM Assembly



Note: The PHM assembly is shown with narrow retention mechanism and heatsink.

1.3 References

Material and concepts available in the following documents may be beneficial when reading this document.

Table 1-1. Reference Documents

Document Title	Reference Number	Notes
Second Generation Intel® Xeon® Scalable Processors Datasheet Volume One: Electrical	338845	
Second Generation Intel® Xeon® Scalable Processors Datasheet Volume Two: Registers	338846	
Second Generation Intel® Xeon® Scalable Processors Specification Update	338848	

1.4 Terminology

Table 1-2. Terms and Descriptions (Sheet 1 of 2)

Term	Description
Bypass	Bypass is the area between a passive heatsink and any object that can act to form a duct. For this example, it can be expressed as a dimension away from the outside dimension of the fins to the nearest surface.
DTS	Digital Thermal Sensor reports a relative die temperature as an offset from TCC activation temperature.
FSC	Fan Speed Control
HTg	Printed circuit board material, such as FR4, with high glass transition temperature
IHS	Integrated Heat Spreader: a component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
LEC54B	54 Pin high speed low loss edge connector design specifically for Intel processors
LGA3647 Socket	Surface mounted socket with 3647-contacts enabling the processor to interface with the system board
Margin to $T_{CONTROL}$	Least margin based on each die type with a $T_{CONTROL}$
Margin to Throttle	Least margin based on each die type
Pad Crater	Mechanically induced fracture in the resin between copper foil and outermost layer of fiberglass of a printed circuit board
PECI	The Platform Environment Control Interface (PECI) is a one-wire interface that provides a communication channel between the Intel processor and the chipset components to the external monitoring devices.
PHM	Processor Heatsink Module - An assembly of processor and heatsink
PHLM	Processor Heatsink Load Mechanism
Ψ_{CA}	Case-to-ambient thermal characterization parameter. A measure of thermal solution performance. Defined as $(T_{CASE} - T_{LA})$ / Total Package Power. Heat source should always be specified for Ψ measurements.
Ψ_{CS}	Case-to-sink thermal characterization parameter. A measure of thermal interface material performance. Defined as $(T_{CASE} - T_S)$ / Total Package Power.
Ψ_{SA}	Sink-to-ambient thermal characterization parameter. A measure of heatsink thermal performance using total package power. Defined as $(T_S - T_{LA})$ / Total Package Power.
T_{CASE}	The case temperature of the processor measured at the geometric center of the topside of the IHS
T_{CASE_MAX}	The maximum case temperature as specified in a component specification
TCC	Thermal Control Circuit: Thermal monitor uses the TCC to reduce the die temperature by using clock modulation and/or operating frequency and input voltage adjustment when the die temperature is very near its operating limits.
$T_{CONTROL}$	$T_{CONTROL}$ is a static value below TCC activation that is used as a trigger point for fan speed control. When DTS > $T_{CONTROL}$, the processor must comply to the thermal profile.
TDP	Thermal Design Power: Thermal solution should be designed to dissipate this target power level. TDP is not the maximum power that the processor can dissipate.
Thermal Monitor	A power reduction feature designed to decrease temperature after the processor has reached its maximum operating temperature
Thermal Profile	A line that defines the case temperature specification of a processor at a given power level.
TIM	Thermal Interface Material: The thermally conductive compound between the heatsink and the processor case. This material fills the air gaps and voids, and enhances the transfer of the heat from the processor case to the heatsink.

Table 1-2. Terms and Descriptions (Sheet 2 of 2)

Term	Description
T_{LA}	The measured ambient temperature locally surrounding the processor. The ambient temperature should be measured just upstream of a passive heatsink or at the fan inlet for an active heatsink.
T_{SA}	The system ambient air temperature external to a system chassis. This temperature is usually measured at the chassis air inlets.
U	A unit of measure used to define server rack spacing height. 1U is equal to 1.75 in, 2U equals 3.50 in., and so forth.

§

2 Processor Package Mechanical Specification

This section provides an overview of the processor package mechanical design and integration. The package serves as the primary interface between the processor silicon die and the rest of the system. The package provides electrical signaling and power delivery as well as thermal transmission, mechanical physical attach, dimensional scale translation and structural strength and stiffness. A solid understanding of the processor design targets provides the necessary foundation to identify and establish thermal and mechanical design requirements for the motherboard and the system.

To ensure compatibility with the processor and the platform, the mechanical processor retention and thermal solution must meet the requirements and keep out zones of both the processor and the LGA3647-0 socket. This section provides the processor package specific mechanical specifications and handling guidance.

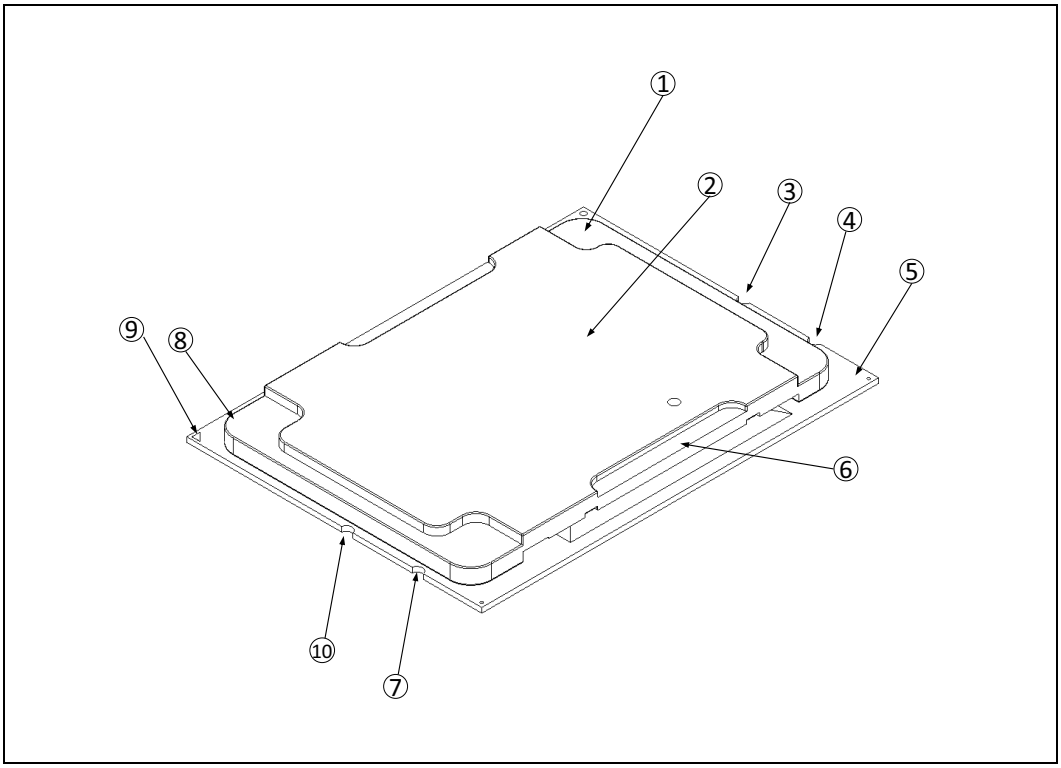
2.1 Processor Package Description

The processor is housed in an Flip-Chip Land Grid Array (FC-LGA14) package that interfaces with the motherboard via an LGA3647-0 SMT socket. The package consists of a processor Integrated Heat Spreader (IHS), which is attached to the package substrate and die and serves as the mating surface for the processor component thermal solutions, such as a heatsink. The IHS transfers the non-uniform heat from the die to the top of the IHS, out of which the heat flux is more uniform and spread over a larger surface area (not the entire IHS area). This allows more efficient heat transfer out of the package to an attached cooling device. The IHS is designed to be the interface for contacting a heatsink.

Processor package dimension includes an IHS. The bottom side of the package has 3647 lands in a 43.18 x 50.24 mm pad array which interfaces with the LGA3647-0 SMT socket. Regardless of the package form factor of the Second Generation Intel® Xeon® Scalable Processors 2S with two Intel® Ultra Path Interconnects (Intel® UPI), and Second Generation Intel® Xeon® Scalable Processors with three Intel® UPI SKUs are compatible with the LGA3647-0 SMT socket. Mechanical compatibility with the socket is controlled through a predefined package to socket keying size and location. The following figure shows a sketch of the processor package components and how they are assembled together.

Note: The processor package actual land count is greater than the socket contact count. The 137 additional pads are reserved for use during the manufacturing process.

Figure 2-1. Processor Assembly - ISO View



The next package illustrations include the following features:

1. Integrated Heat Spreader (IHS) - Step
2. Integrated Heat Spreader (IHS) - Top Surface
3. PHM package carrier keying slot
4. Socket keying slot
5. Processor package substrate
6. Integrated Heat Spreader (IHS) - Step
7. Socket keying slot
8. Integrated Heat Spreader (IHS) - Step
9. Pin 1 indicator
10. PHM package carrier latch slot

2.2 Processor Mechanical Dimensions

The processor package mechanical drawings are referenced in Appendix B. They include dimensions necessary to design a thermal solution for the processor. These dimensions include:

1. Package reference dimensions with tolerances (total height, length, width, and so on)
2. IHS parallelism and tilt
3. Land dimensions
4. Top-side and back-side component keep-out dimensions
5. Reference datum

2.3 Processor Keep-Out Zones

The processor contains components on the top and bottom sides of the interposer that define component keep-out zone requirements. A thermal and mechanical solution design must not intrude into the identified keep-out zones. See processor package mechanical drawing for location, size, and additional information on keep-out zones. The location and quantity of package capacitors may change but will remain within the component keep-in areas.

2.4 Processor Mechanical Loads

The processor package has mechanical load limits that should not be exceeded during the processor ILM actuation, heatsink installation and removal, mechanical stress testing, or standard shipping conditions as permanent damage to the processor may occur. For example, when a compressive static load is necessary to ensure thermal performance of the Thermal Interface Material (TIM2) between the heatsink base and the IHS, it should not exceed the corresponding specification. The processor substrate should not be used as a mechanical reference or load-bearing surface for thermal solutions.

Table 2-1 provides load specifications for the processor package. These maximum limits should not be exceeded during heatsink assembly, shipping conditions, or standard use condition. Exceeding these limits during test may result in component failure. The processor substrate should not be used as a mechanical reference or load bearing surface for thermal solutions unless identified within this document.

Table 2-1. Processor Loading Specifications

Parameter	Value	Notes
Max. Allowable Static Compressive Load	1334 N [300 lbf]	2
Max. Allowable Dynamic Compressive Load	588 N [132 lbf]	1, 2, 3

Notes:
1. Duration of the load does not to exceed one second (1 s).
2. These specifications apply to uniform compressive loading in the direction normal to the processor IHS.
3. Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement.
4. Through the life of product. The condition must be satisfied at the beginning of life and at the end of life.
5. Loads include coupling load for 0.6 kg HS in 3.13 gRMS.

The heatsink will also add an additional dynamic compressive load to the package during a mechanical shock event. Amplification factors due to the impact force during shock must be taken into account in dynamic load calculations. The total combination

of dynamic and static compressive load should not then exceed the processor compressive dynamic load during a vertical shock. Using any portion of the processor substrate as a load-bearing surface in either static or dynamic compressive load conditions is not recommended.

2.4.1 Processor Component Keep-Out Zones

The processor may contain components on the substrate that define component keep-out zone requirements. A thermal and mechanical solution design must not intrude into the required keep-out zones. Do not contact the test pad area with conductive material. Decoupling capacitors are typically mounted to either the topside or land-side of the package substrate. See the processor package mechanical drawing for location, size, and additional information on keep-out zones. The location and quantity of package capacitors may change due to manufacturing efficiencies but will remain within the component keep-in areas.

2.4.1.1 Processor Materials

Table 2-2 lists some of the package components and associated materials.

Table 2-2. Processor Materials

Component	Material
Integrated Heat Spreader (IHS)	Nickel Plated Copper
Substrate	Halogen Free, Fiber Reinforced Resin
Substrate Lands	Gold Plated Copper

2.5 Processor Mass Specification

The typical mass of the processor is 112 grams. This mass includes all the components that are included in the package.

2.6 Package Insertion Specifications

Table 2-3. Package Interface Requirement

Socket Insertion	The processor can be inserted into and removed from an LGA3647-0 socket 30 times.

2.7 Processor Markings

Figure 2-3 shows the topside markings on the processor. This diagram is to aid in the identification of the processor.

Figure 2-2. Second Generation Intel® Xeon® Scalable Processors Package Topside Markings

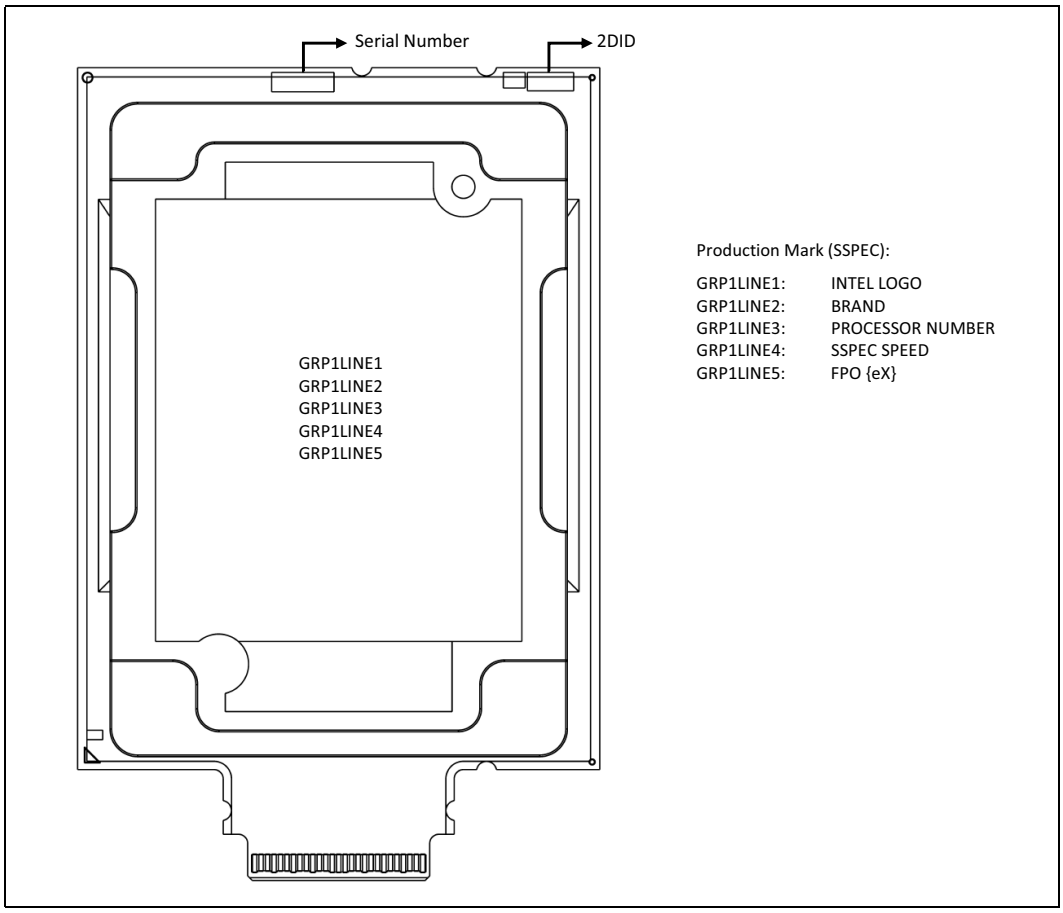


Figure 2-3. Second Generation Intel® Xeon® Scalable Processors Package Bottom Side Markings

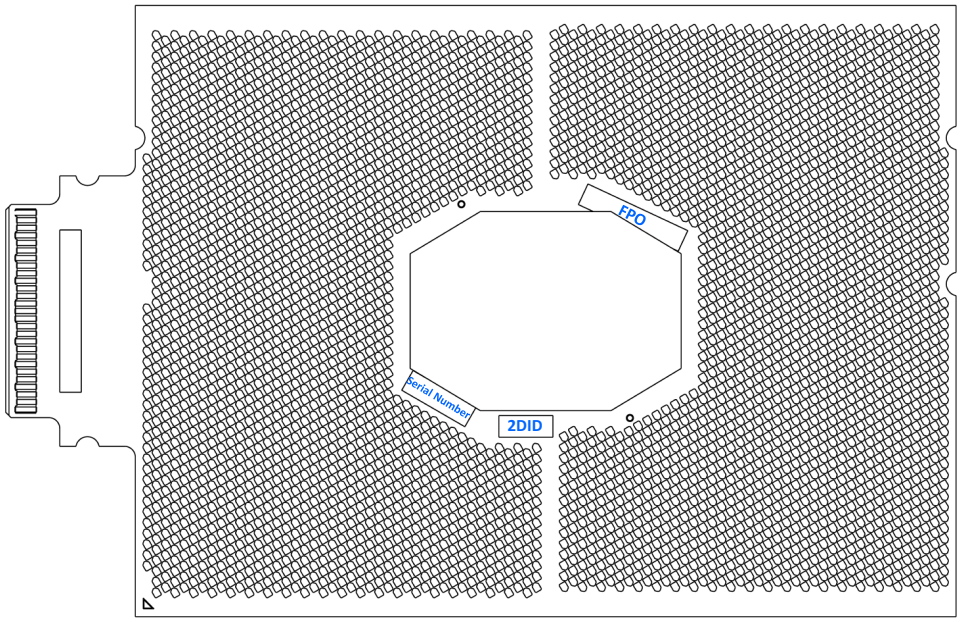


Table 2-4. Processor Mark Definition

Mark	Definition
QDF_SPEED	Product Specification Number and Speed
SN345	Serial Number (5 digit)
FPO45678_{eX}	Lot Number (8 digit) - eX
2D	2D Matrix Mark

2.7.1 Package Handling Guidelines

The processor package may contain components on the top or bottom sides of the interposer. To remove the processor from its shipping container or the tray, grab and hold the processor along its long edges.

Note: Avoid contacting the processor bottom side lands and/or gold fingers.

When installing the processor into the socket, care should be taken to ensure that the processor is properly oriented, that is the processor pin-1 is in the same direction as the socket pin-1, and that there are no contaminations or foreign material on the land pads or gold fingers.

In a case where the processor is not installed into the socket, it should be placed or stored in the appropriate tray or container as to avoid damaging the package interposer or its bottom side components.

§

3 Socket Specifications

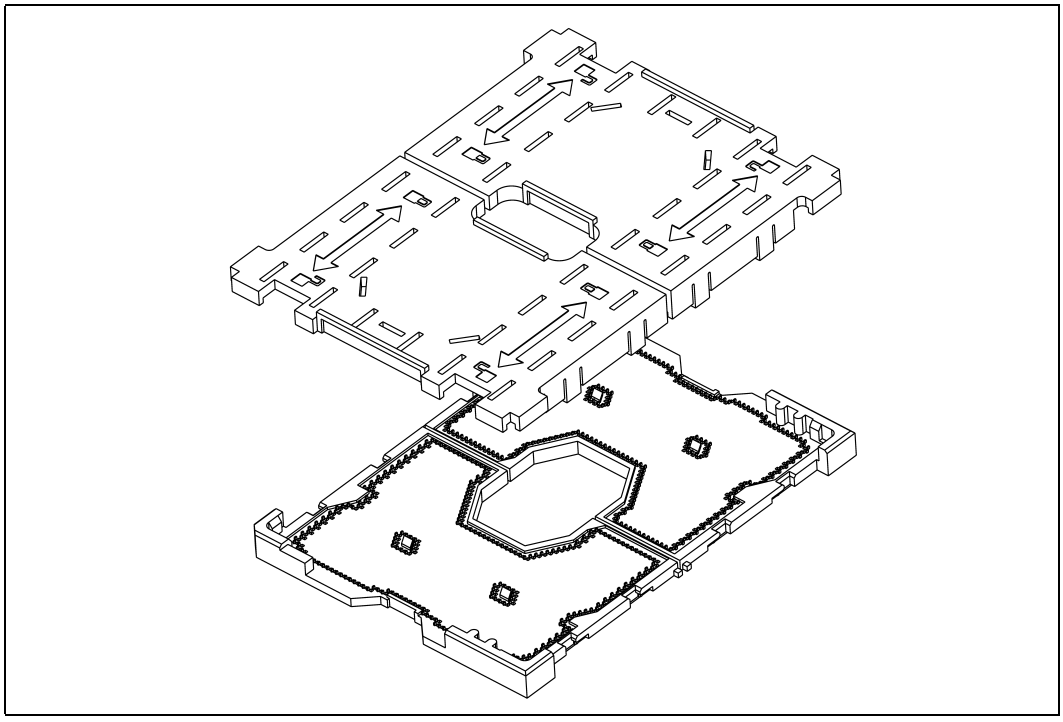
This section describes the LGA3647-0 surface mount Land Grid Array (LGA) socket. The socket contains a total of 3647 contacts and provides I/O, power, and ground connections from the main board to the processor package.

The socket definitions listed intend to identify the minimum socket requirements and features necessary to ensure compatibility with the Second Generation Intel® Xeon® Scalable Processors and the Second Generation Intel® Xeon® Scalable Processors based platform. In addition to these, socket suppliers may include design features to ensure their socket design meets Intel specifications as well as their manufacturing process requirements. See the supplier listing for ordering and contacting information.

3.1 Socket Overview

The LGA3647-0 socket is made-up of two sections. Each section of the socket consist of the socket body and the Pick and Place (PnP) cover. The two halves are not interchangeable and are distinguishable from one another by the colors of the keying features: yellow for one half and black for the other. They are delivered by the socket supplier as a single integral assembly. The main body of the socket, which is made of electrically insulated material with resistance to high temperature, houses the socket contacts. Figure 3-1 illustrates the socket features. Keying features (wall protrusions) within the contact array area and raised edges of the socket body help align the package with respect to the socket contacts.

Figure 3-1. LGA3647-0 Socket with PNP Capacitor



Note: Picture shown is of a generic LGA3647 socket. See socket drawing for feature details such as package keying associated with the LGA3647-0 socket.

Figure 3-2. LGA3647-0 Socket with PNP Capacitor Post SMT Process

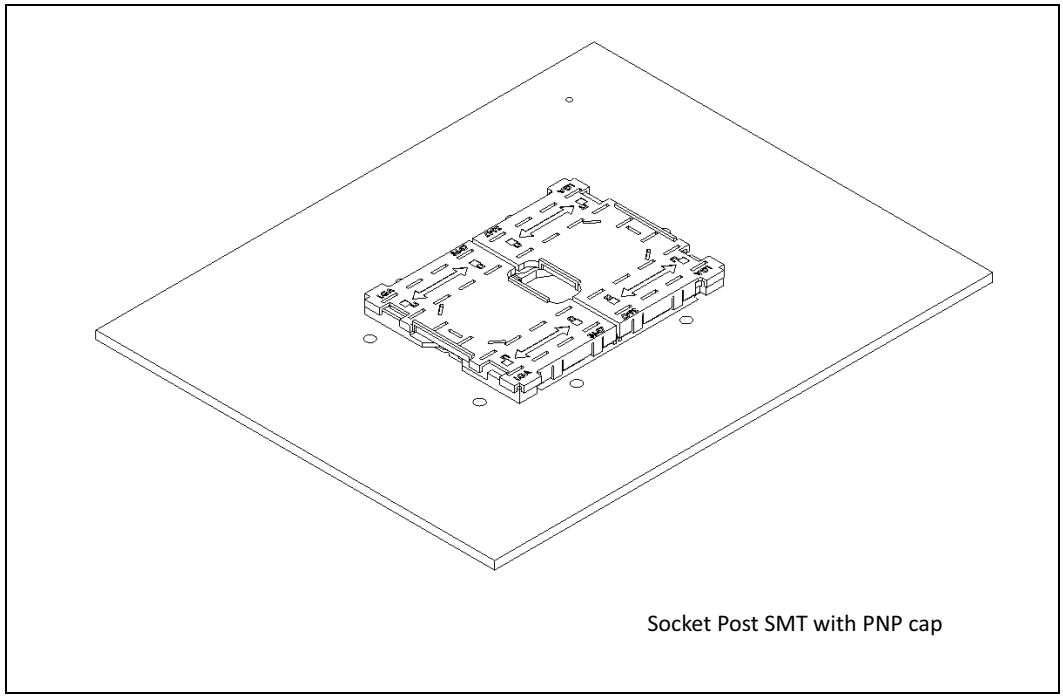


Figure 3-3. LGA 3647-0 Socket (Right Side)

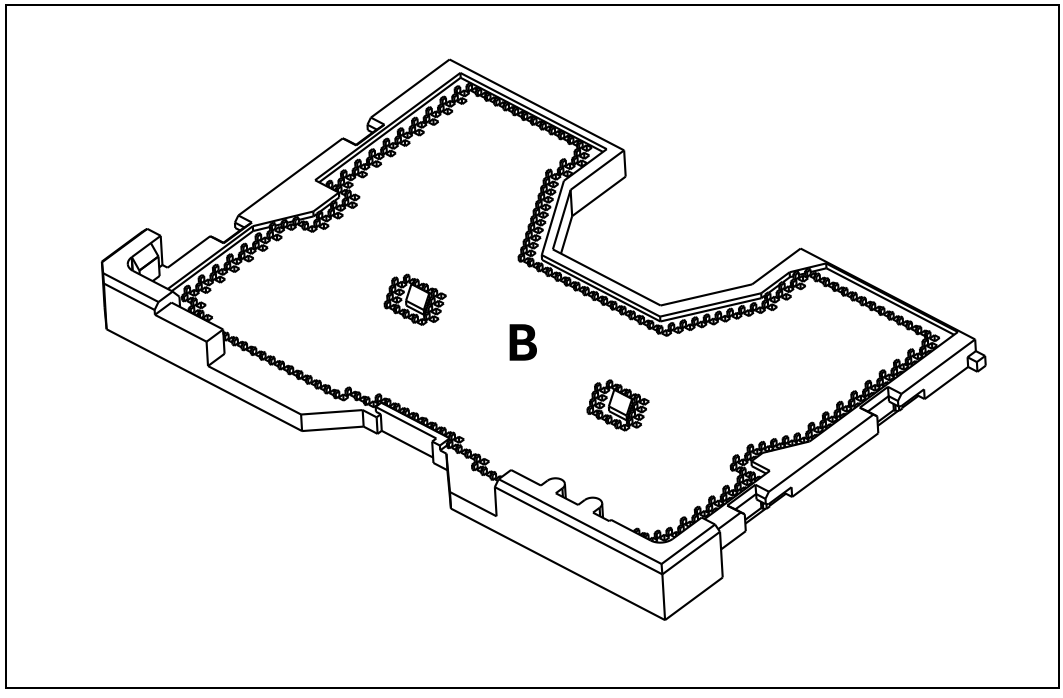
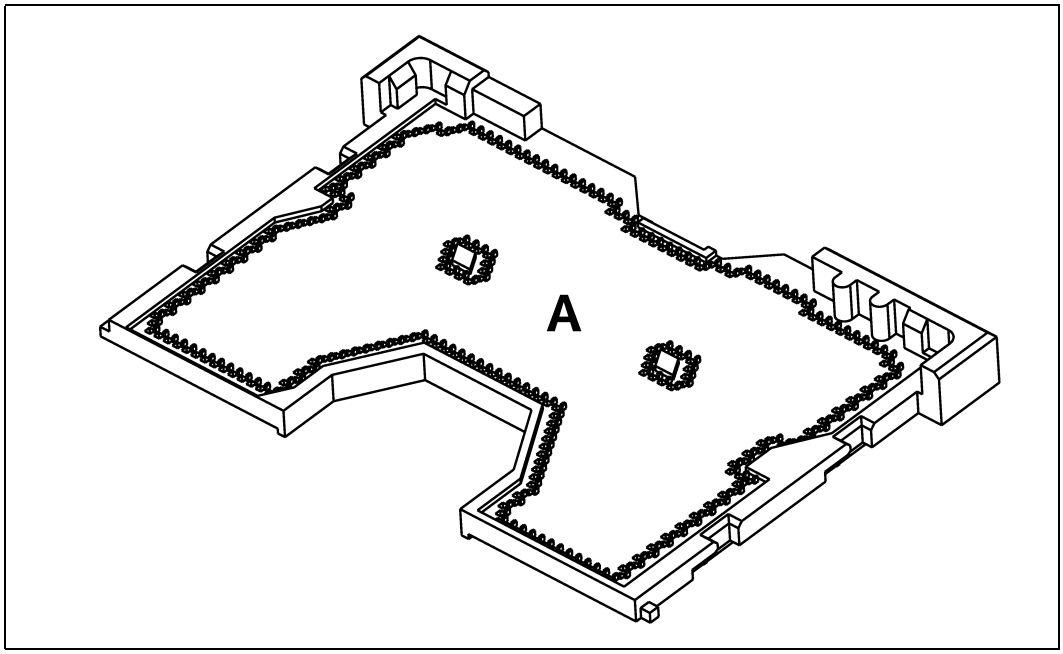


Figure 3-4. LGA 3647-0 Socket (Left Side)



Note: Socket contacts are not shown.

Table 3-1. Socket Features Attribute

Socket Feature	Attributes	Notes
Socket wall exterior dimensions	82 mm x 62 mm	As measured post assembly and includes both sections of the socket
Socket wall Interior dimensions	76.11 mm x 56.6 mm	
Solder ball pitch	0.86 mm (X) x 0.99 mm (Y)	Hexagonal pattern
Ball count	3647	Not all socket contacts are assigned to a processor signal. Some are reserved or are considered NCTF.

The socket interfaces with the Processor Heatsink Module (PHM). Socket loading is achieved through locking down the PHM to the PHLM. Uniform load on the socket solder joints is achieved through the backplate held to the motherboard secondary side.

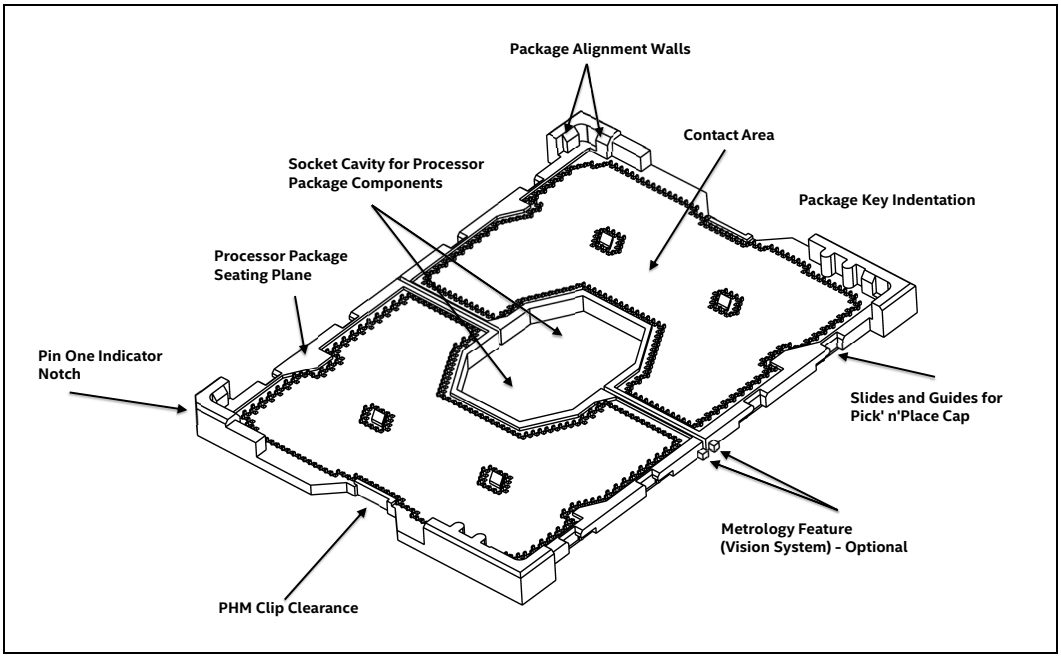
The socket cover is intended to be reusable and recyclable. It will enable socket pick and placing during motherboard assembly. The socket cover will also protect the socket contacts from contamination and damage during board assembly and handling.

3.2 Socket Features

The LGA3647 socket is made of two sections, right (B) and left (A) sides. Sections are similar, but not identical. Key differences between the sections are the locations of the package keying. Care should be taken to ensure package keying matches the LGA3647-0 socket.

Key features of the LGA3647 socket include contact array, socket cavity, package keying, side walls, package seating plane, slides and guides for the pick and place capacitor, and the clearance for the PHM package carrier.

Figure 3-5. LGA3647-0 Mechanical Features



3.3 Socket Housing

3.3.1 Housing Material

The socket housing material should be thermoplastic or equivalent, UL 94 V-0 flame rating, temperature rating and design capable of maintaining structural integrity following a temperature of 260 °C for 40 seconds, which is typical of a reflow/rework profile for solder material used on the socket. The material must have a thermal coefficient of expansion in the XY plane capable of passing reliability tests rated for an expected high operating temperature, mounted on HTg FR4-type motherboard material.

The material of socket housing is required to have minimum yield strength of 35 MPa at 90 °C to minimize the risk of seating plane deformation.

The creep properties of the material must be such that the mechanical integrity of the socket is maintained for the stress conditions outlined in Appendix A.

3.3.2 Housing Color

The color of the socket housing must be dark as compared to the solder balls to provide the contrast needed for OEM's pick and place vision systems. Components of the socket may be different colors as long as they meet the previous requirement.

3.3.3 Package Installation/Removal Access

Access must be provided to facilitate the manual insertion and removal of the package. No tool should be required to install or remove the package from the socket.

3.3.4 Package Alignment/Orientation

A means of providing fixed alignment and proper orientation with the pin 1 corner of the package must be provided. There are three different levels of package alignment:

- The first level is called gross alignment, which happens between PHM and the posts on the bolster plate.
- The second level is called intermediate alignment, which utilizes the socket exterior corner walls and package clip.
- The third level, which is fine alignment, relies on the socket inner wall surfaces.

The socket also has orientation posts or protrusions (keys) placed on opposite sides of the socket as noted in Appendix C. The package substrate will have keying notches at the corresponding locations. When package keying notches align with socket orientation posts, it prevents th package from being mistakenly installed with a 180 degree in-plane rotation. The package will sit flush on the socket contacts when aligned.

3.3.5 Heatsink Retention and Processor Package Carrier Compatibility

A direct keying feature between the bolster plate and LGA3647-0 socket does exist. Keying is achieved through the board hole pattern for the bolster plate which is defined specifically for LGA3647-0 compatible bolster plates (narrow and square). During board assembly special attention should be given to the bolster plate part number and the processor package keying on the socket.

Two cutouts on the ends of socket provides clearance for the PHM package carrier-package latch feature. In addition, the PHM package carrier utilizes the socket side walls as the pre-alignment between the socket and processor.

3.3.6 Markings

All markings required in this section must withstand a temperature of 260 °C for 40 seconds, which is typical of a reflow/rework profile for solder material used on the socket, as well as any environmental test procedure outlined in Appendix A, without degrading. Socket marks must be visible after it is mounted on the motherboard.

- Name:

LF-LGA3647-0 (font type is Helvetica Bold – minimum 4 point [or 1.411 mm])

Note: This mark shall be molded or laser marked as shown in Appendix C.

Manufacturer's Insignia (font size at supplier's discretion).

This mark will be molded or laser-marked into the top side of the socket housing.

Both socket name and manufacturer's insignia must be visible when first seated on the motherboard.

- Lot Traceability

Each socket will be marked with a lot identification code to allow traceability of all components, date of manufacture (year and week), and assembly location. The mark must be placed on a surface that is visible after the socket is mounted on the motherboard. In addition, this identification code must be marked on the exterior of the box in which the unit is shipped.

- Visual Aids

The socket must have pin A1 and package/socket alignment keys.

3.3.7 Contact Characteristics

Number of Contacts

Total number of contacts: 3647

Layout

The contacts are laid out in two "C" shape regions opposing each other. The arrows in the figure indicate the wiping orientation of the contacts in the two regions to be 60° about the horizontal axis. There are 1823 and 1824 contacts in the right and left halves of the socket, respectively.

Base Material

High-strength copper alloy.

Contact Area Plating

For the area on socket contacts where processor lands will mate, there is either a 0.762 µm [30 µ-inches] or 0.381 µm [15 µ-inches] gold plating over 1.27 µm [50 µ-inches] minimum nickel under plating in critical contact areas (area on socket contacts where processor lands will mate) is required. No contamination by solder in the contact area is allowed during solder reflow.

Lubricants

For the final assembled product, no lubricant is permitted on the socket contacts. If lubricants are used elsewhere within the socket assembly, these lubricants must not be able to migrate to the socket contacts.

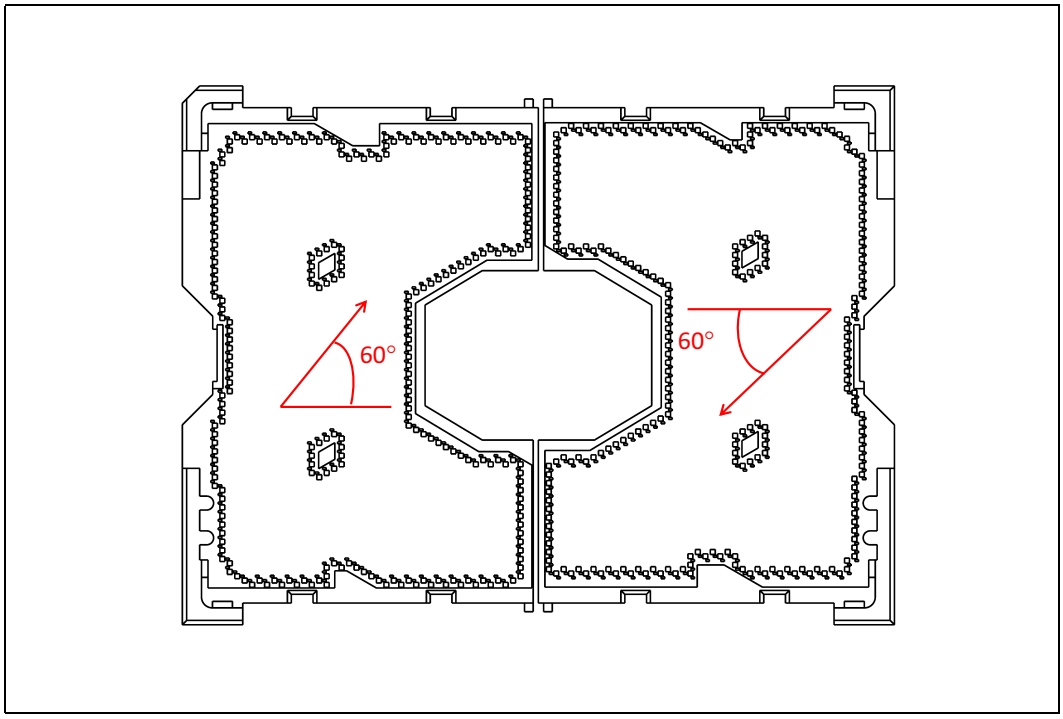
Co-Planarity

The co-planarity (profile) requirement for all contacts mating to the top side of the socket is defined in the socket drawing.

True Position

The contact pattern has a true position requirement with respect to applicable datum in order to mate with the package land pattern.

Figure 3-6. Contact Orientation



Stroke/Load

The minimum vertical height of the contact above the package seating plane is defined in the socket drawing. The minimum vertical stroke of the contact must, under all tolerance and warpage conditions, generate a normal force load to ensure compliance with all electrical requirements of the socket. The cumulative normal force load of all contacts must not exceed the load limits.

3.3.8 Contact/Pad Mating Location

The offset between processor package LGA land center and solder ball center is defined in the following figure. All socket contacts should be designed such that the contact tip does not damage solder resist, defining the LGA land during actuation and remains within the substrate pad boundary as illustrated. All sockets must also not interfere with solder resist at minimum static compressive load per contact and at final installation after actuation load is applied. This requirement includes all the X-Y tolerances such as socket size, substrate size, and pad true positional tolerance, as defined in socket drawings. Also it is recommended that the contact tip remains within the substrate pad before any actuation load is applied.

Figure 3-7. LGA3647-0 Socket BGA to Package Pad Offset

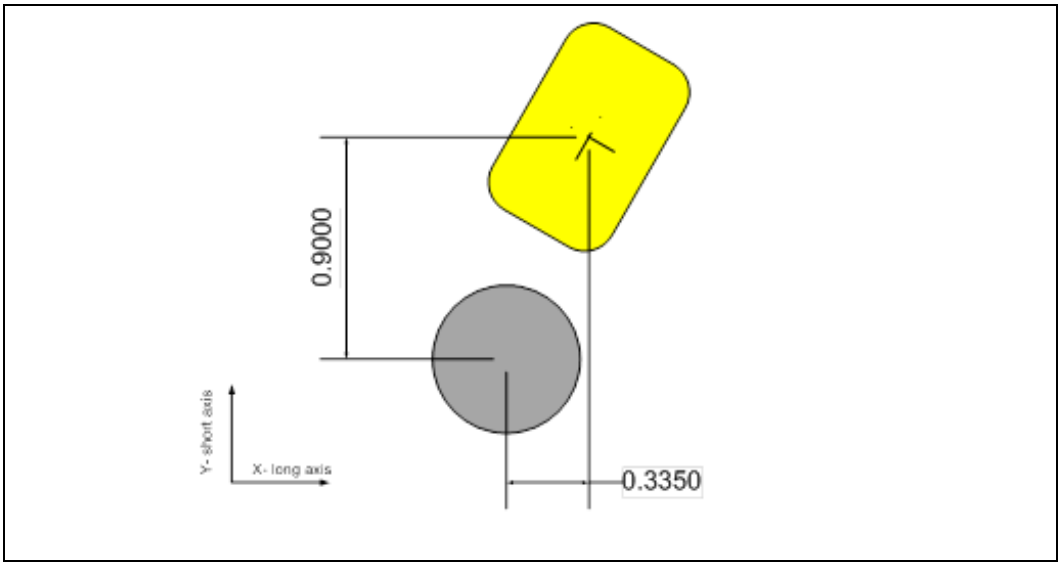
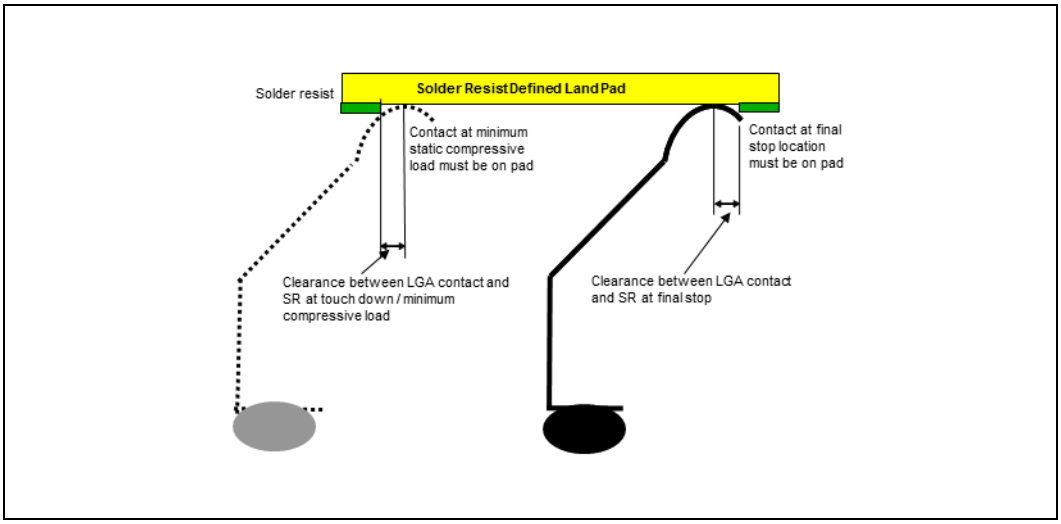


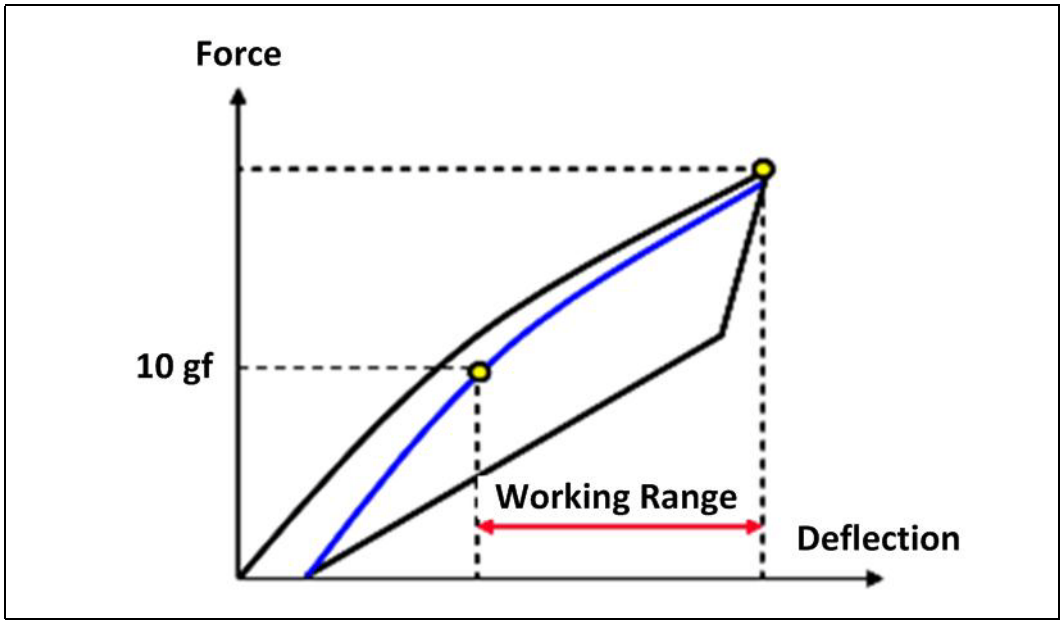
Figure 3-8. Clearance Between Solder Resist and Socket Contact Tip



3.3.9 Contact-Deflection Curve

The contact should be designed with an appropriate spring rate and deflection range to ensure adequate contact normal force in order to meet EOL performance at all contact locations. The load-deflection curve is not necessary to be linear between the minimum and maximum deflection points. The LGA contact working range is defined as the difference of contact deflection at the minimum contact load and the maximum contact deflection.

Figure 3-9. Contact Deflection Curve



3.3.10 Solder Ball Characteristics

Number of Solder Balls

Total number of solder balls: 3647

Layout

The solder balls are laid out in two “C” shape regions, see socket drawing for details.

Material

Lead free SAC solder alloy with a silver content between 3% and 4% with a melting point temperature of 217 °C maximum (for example, SnAgCu) and is compatible with standard lead free processing such as Immersions silver (ImAg) and OSP MB surface finish with SnAg/SnAgCu solder paste.

Co-Planarity

The co-planarity (profile) requirement for all solder balls on the underside of the socket is defined in the socket drawing.

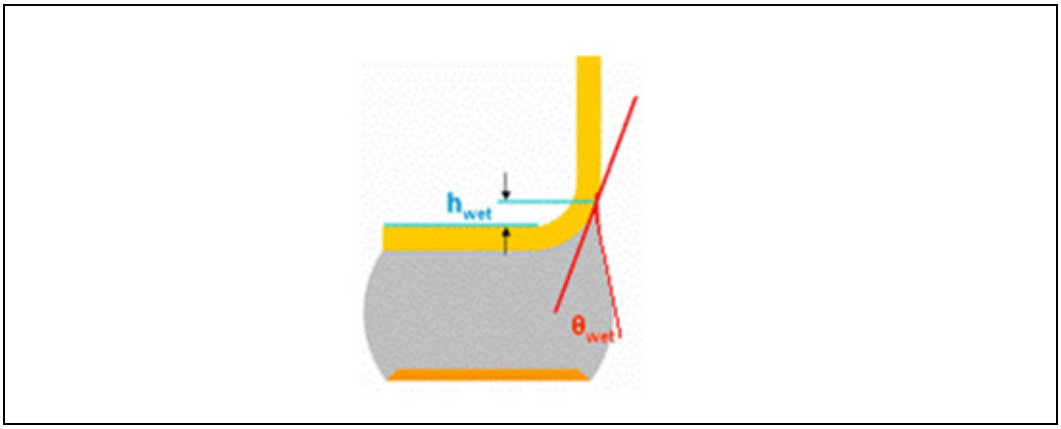
True Position

The solder ball pattern has a true position requirement with respect to applicable datum in order to mate with the motherboard land pattern. Refer to the socket drawing for details.

Solder Ball Wetting Angle

To minimize the risk associated with shock, vibration, and transient bend stresses, the solder ball wetting angle must be controlled via ball attach process optimization such that the post SMT wetting angle, as defined in Figure 3-10, is less than or equal to 90 degrees. In the event that a correlation can be identified between wetting height and wetting angle, the wetting height may also be used as a measurable success criterion.

Figure 3-10. Solder Ball Wetting Angle and Height



3.4 Socket Mechanical Requirements

3.4.1 Socket Size

The socket should meet the dimensions provided in the Appendix C.

3.4.2 Socket Standoffs

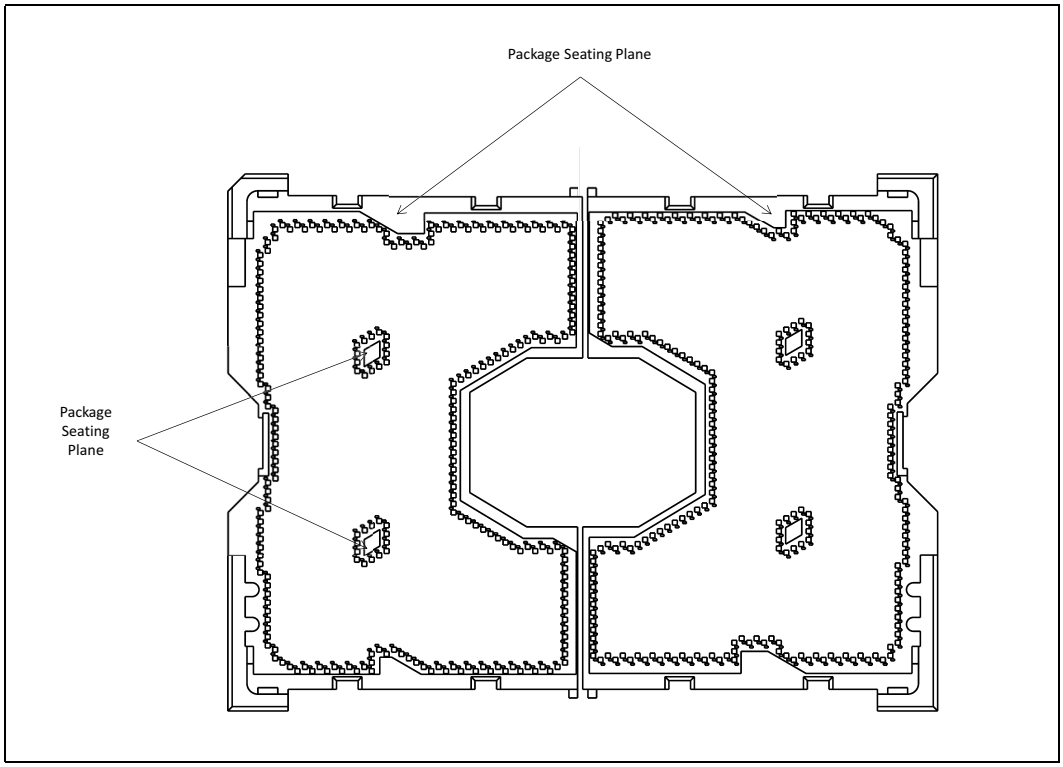
Standoffs must be provided on the solder ball side of the socket base to ensure the minimum socket height after solder reflow and to prevent socket housing over deflection after being loaded. It is required that wherever there is a top side primary socket seating plane for package, there should be a corresponding standoff on the bottom side. A gap between the solder-ball seating plane and the standoff prior to reflow is required to ensure sufficient ball collapse during surface mount.

3.4.3 Package Seating Plane

The socket seating plane for the package defines the minimum package height from the motherboard. See the processor mechanical drawing for details on package and IHS height above the motherboard. The datum is defined by the top surfaces of seating plane standoffs which cause a hard stop of package over the socket when the package and socket are loaded. There are primary socket seating planes and secondary socket seating planes.

- Primary seating planes are located at areas where contacts are depopulated and around socket cavity and center split location as illustrated.
- Secondary seating planes are interstitial seating planes, which are small islands within a pitch range and around each core pin except for manufacturing keep-outs.

Figure 3-11. LGA364-x Package Seating Plane



Both primary and secondary seating plane area and numbers of the seating planes are maximized to avoid significant creep of the housing material when being loaded; however, the seating plane standoffs should not touch the LGA lands on the bottom of the package. It is recommended that the nominal height of interstitial seating plane be the same as the nominal height of primary seating planes, but the highest points of interstitial seating planes must be no higher than the highest points of primary socket seating planes. The seating plane co-planarity needs to meet the specification after socket surface mount.

3.4.4 Package Translation

The socket should be built so that the post-actuated seating plane of the package is flush with the seating plane of the socket. Movement will be along the axis normal to the seating plane.

3.4.5 Insertion/Removal/Actuation Forces

Any actuation must meet or exceed SEMI S8-95 Safety Guidelines for Ergonomics/ Human Factors Engineering of Semiconductor Manufacturing Equipment, example Table R2-7 (Maximum Grip Forces).

Access must be provided to facilitate the manual insertion and removal of the package. The socket must be designed so that it requires no force to insert the package into the socket. No tool should be required to install or remove the package from the socket.

3.4.6 Orientation in Packaging, Shipping, and Handling

Packaging media needs to support high-volume manufacturing. Media design must be such that no component of the socket (solder balls, contacts, housing, and so on) is damaged during shipping and handling. Each part number will be shipped from suppliers in separate Joint Electron Device Engineering Council (JEDEC*) trays; for example, all left halves of the socket in 1 tray and all right halves in another. Tray height could be taller than standard.

3.4.7 Pick and Place and Handling Cover

To facilitate high-volume manufacturing, the socket should have a detachable cover to support the vacuum type pick and place system. The cover will remain on the socket during reflow to help prevent contamination. The cover can withstand 260 °C for 40 seconds (typical reflow/rework profile) and the conditions listed without degrading. The cover could also be used as a protective device to prevent damage to the contact field during handling.

Cover retention must be sufficient to support the socket weight during lifting, translation, and placement, during board manufacturing, and throughout board and system shipping and handling. The cover design should allow use of a tool to remove the cover. The force required for removing of the cover should meet or exceed the applicable requirements of SEMI S8-0999 Safety Guidelines for Ergonomics/Human Factors Engineering of Semiconductor Manufacturing Equipment. The removal of the cover should not cause any damage to the socket body nor to the cover itself within the cover durability limit.

The pick and place cover should provide a viewing window to make the pin A1 indicator visible on the underlying socket.

Table 3-2. Socket PnP Cover Insertion/Removal

Direction	Condition	Value	Note
In plane	Removal	0.77 kgf [1.7 lbf] max.	Pinch Grip Orientation
In and Out Plane	Shock	0.36 kgf [0.8 lbf] min.	Shipping condition
Vertical	Closed position at 260 °C	0.34 kgf [0.75 lbf] min.	• To support socket vertical lift-off during SMT process • PnP cover shall not fall-off in rework
	Closed position at room temperature	0.34 kgf [5.0 lbf] min. 10 kgf [22.0 lbf] max.	

3.4.8 Durability

The socket must withstand 30 cycles of processor insertion and removal. The maximum part average and single pin resistance from Appendix G, "Board Flexure Initiative" must be met when mated in the first and 30th cycles.

3.4.9 Socket Keep-In/Keep-Out Zone

Socket keep-in and keep-out zones are identified on the motherboard to ensure that sufficient space is available for the socket, and to prevent interference between the socket and the components on the motherboard. These areas are illustrated in board volumetric keep-outs for the socket. It is the responsibility of the socket supplier and the customer to identify any required deviation from specifications identified here.

3.4.10 Attachment

The socket will be attached to the motherboard via its 3647 solder balls. There are no additional external methods (that is, screw, extra solder, adhesive, and so on) to attach the socket.

The socket will be tested against the mechanical shock and vibration requirements under the expected use conditions with all assembly components under the loading conditions.

3.4.11 Socket Loading and Deflection Specifications

The socket must meet the mechanical loading and strain requirements outlined in the following table. These mechanical load limits should not be exceeded during component assembly, mechanical stress testing, or standard drop and shipping conditions. All dynamic requirements are under room temperature conditions while all static requirements are under 125 °C conditions.

Table 3-3. Socket Loading and Deflection Specifications

Parameter	Values		Notes
	Min.	Max.	
Static Compressive Load Per Contact	10 gf	25 gf	1
Total Package Static Compressive Load	BOL: 801 N [180 lbf]	BOL: 1334 N [300 lbf]	2, 7
	EOL: 614 N [138 lbf]	EOL:1334 N [300 lbf]	2
Dynamic Compressive Load	N/A	588 N [132 lbf]	4, 5
Board Transient Bend Strain	62 to 72 mil board thickness	500 µs (MicroStrain)	3, 6
	93 to 130 mil board thickness	450 µs (MicroStrain)	

Notes:
1. The compressive load applied on the LGA contacts to meet electrical performance.
2. The total compressive load applied by the heatsink onto the socket through the processor package.
3. Maximum allowable strain below socket BGA corners during transient loading events (i.e., slow displacement events) which might occur during board manufacturing, assembly or testing. See the *LGA3647 Board Flexure Initiative (BFI) Strain Guidance Sheet*. Contact your CQE for this datasheet.
4. Dynamic compressive load applies to all board thicknesses.
5. The quasi-static equivalent compressive load applied during the mechanical shock. Dynamic compressive limit has been calculated using the assumption of 2x dynamic amplification factor at processor location using a 600 gm heat sink and a 50 G table input. The product application can have flexibility in specific values, but the ultimate product of mass times acceleration times corresponding amplification factor should not exceed this dynamic compressive load limit. Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement. This load is superimposed onto the socket static compressive load to obtain total dynamic load.
6. Board transient bent strain limits apply only to board manufacturing process steps such as ICT. It is not for substitute for shock and vibration. Maximum allowable strain at the socket BGA corners during transient loading events, such as slow displacement events, which might occur during board manufacturing, assembly, or testing. See the *LGA3647-1 Board Flexure Initiative (BFI) Strain Guidance Sheet*. Contact your manufacture Certified Quality Engineer (CQE) representative for this datasheet.
7. The minimum Total Static Compressive Load (BOL) specification only applies to the processor with fabric. The processor without fabric only requires that the minimum Total Static Compressive Load (EOL) be met over its lifetime (Only fabric processors are present in the first generation).

The minimum *Static Total Compressive* load will ensure socket reliability over the life of the product and that the contact resistance between the processor and the socket contacts meets the values outlined in the previous table.

3.4.12 Socket Critical-to-Function Interfaces

Critical-to-function (CTF) dimensions for the motherboard layout and the assembled components interface to the socket are identified in the socket drawing. All sockets manufactured must meet the specified CTF dimensions.

3.5 Material and Recycling Requirements

Cadmium should not be used in the painting or plating of the socket.

Chlorofluorocarbon Compounds (CFC) and Hydrofluorocarbon Compounds (HFC) should not be used in manufacturing the socket.

Components should comply with recycling standards (e.g., European Blue Angel), and must comply with environmental legislation including those related to restrictions on the use of lead and bromine containing flame-retardants. Legislation varies by geography; European Union (RoHS/WEEE), China, California, etc.

3.6 LGA3647 Socket Land Pattern

Solder balls enable the socket to be surface mounted to the processor board. Each contact will have a corresponding solder ball. Solder ball position may be at an offset with respect to the contact tip and base. Hexagonal area array ball-out increases contact density by 12% while maintaining 39 mil minimum via pitch requirements.

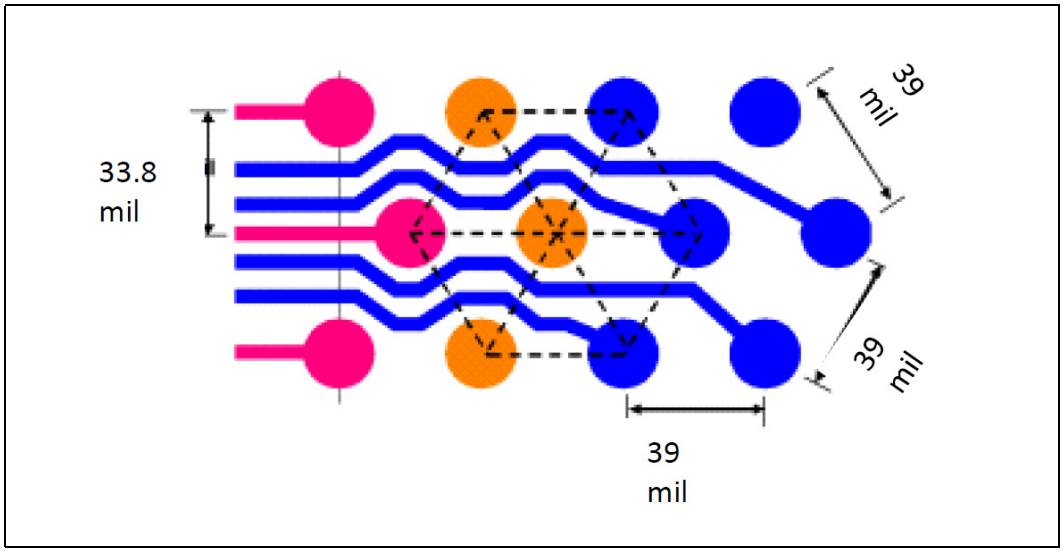
Contact Pattern

LGA3647-0 socket contacts are in 1.0 mm (0.039”) hexagonal pitch in a 105 x 43 grid array with depopulated section in the center of the array and selective depopulation elsewhere. See the socket drawing for details. The tips of the contacts will extend beyond the surface of the socket to make contact with the pads located at the bottom of the processor package.

BGA Pattern

The land pattern for the LGA3647 socket is a 39 mil hexagonal array. For CTF joints, the pad size will primarily be a circular Metal Defined (MD) pad and these pads should be designated as a critical dimension to the PCB vendors with a 17 mil ±1 mil tolerance. Some CTF pads will have an SMD pad (20 x 17 mil).

Figure 3-12. LGA3647-0 Socket PCB Land Pattern



3.7 Strain Guidance for Socket

Intel provides manufacturing strain guidance commonly referred to as Board Flexure Initiative or BFI Strain Guidance. The BFI strain guidance applies only to transient bend conditions seen in a board manufacturing assembly environment, for example during in circuit test. BFI strain guidance limits do not apply once PHM is installed. It should be noted that any strain metrology is sensitive to boundary conditions. Intel recommends the use of BFI to prevent solder joint defects from occurring in the test process. For additional guidance on BFI, see *Manufacturing With Intel® Components - Strain Measurement for Circuit Board Assembly*, also referred as BFI Manufacturing Advantage Services (MAS) and BFI Strain Guidance Sheet (LGA3647-0 Socket). Consult your Intel Customer Quality Engineer for additional guidance in setting up a BFI program in your factory.

Note: When the PHM is installed onto the board, the boundary conditions change, and the BFI strain limits are not applicable. The PHM, by design, increases stiffness in and around the socket and places the solder joints in compression. Intel does not support strain metrology with the ILM assembled.

§

4 Package and Socket Stack

This section describes the mechanical specification of a processor and socket loading mechanism, and design considerations. This specifications applies to the processor loading mechanism in maintaining its interface with the socket and encompasses the processor thermal solution and its retention mechanism.

Any thermal mechanical design using some of the reference components in combination with any other thermal mechanical solution needs to be fully validated according to the customer criteria. Also, if customer thermal mechanical validation criteria differ from the Intel criteria the reference solution should be validated against the customer criteria.

4.1 Mechanical Load Specification

The processor heatsink module is designed to achieve the minimum socket static pre-load compressive load specification. The minimum static pre-load compressive load is the force provided by the PHM and should be sufficient for rudimentary continuity testing of the socket and/or board. This load value will not ensure normal operation throughout the life of the product.

PHM should apply additional load to achieve the socket static total compressive load. The heatsink load will be applied to the Integrated Heat Spreader (IHS).

Table 4-1 provides load specifications for the PHM. The maximum limits should not be exceeded during assembly, shipping conditions, or standard use condition. Exceeding these limits may result in component failure. The socket body or the processor substrate should not be used as a mechanical reference or load-bearing surface for the thermal solution.

Table 4-1. PHM Load Specification

Parameter	Min.	Max.	Notes
Static Compressive Load	890 N [200 lbf]	1334 N [300 lbf]	1, 2, 4
Dynamic Load	NA	588N [132 lbf]	1, 3
Heatsink Mass	NA	600 g [1.32lb]	
TIM2 Activation Pressure	137.9 kpa [20 psi]		

Notes:
1. These specifications apply to uniform compressive loading in a direction perpendicular to the IHS top surface.
2. These load limits define load limits at the Beginning Of Life (BOL) for the Intel's reference enabling solution to meet the socket End of Life (EOL) loading requirement. PHM load may be different for custom designs. Intel will validate only the stated load distribution. The customer bears the responsibility of verifying the PHM load to ensure compliance with the package and socket loading as well as validating the socket reliability within their system implementation.
3. Dynamic loading is defined as heatsink mass (0.6 kg) x 50g load superimposed for an 11 ms duration average on the static load requirement.
4. Conditions must be satisfied at the Beginning Of Life (BOL), and the loading system stiffness for non-reference designs need to meet a specific stiffness range to satisfy end of life loading requirements.

4.2 Mechanical Design Considerations

A retention/loading mechanism must be designed to support the heatsink because there are no features on the socket on which to directly attach a heatsink. In addition to holding the heatsink in place on top of the IHS, this mechanism plays a significant role in the performance of the system, in particular:

- Ensuring thermal performance of the TIM applied between the IHS and the heatsink. TIMs, especially those based on phase change materials, are very sensitive to applied pressure: the higher the pressure, the better the initial performance. TIMs such as thermal greases are not as sensitive to applied pressure. Designs should consider the possible decrease in applied pressure over time due to potential structural relaxation in enabled components.
- Ensuring system electrical, thermal, and structural integrity under shock and vibration events, particularly the socket solder joints. The mechanical requirements of the attachment mechanism depend on the weight of the heatsink and the level of shock and vibration that the system must support. The overall structural design of the baseboard and system must be considered when designing the heatsink attachment mechanism. Their design should provide a means for protecting socket solder joints, as well as preventing package pullout from the socket.

Note: The load applied by the attachment mechanism and the heatsink must comply with the package specifications, along with the dynamic load added by the mechanical shock and vibration requirements.

Note: The load applied by the attachment mechanism must comply with the processor mechanical specifications, along with the dynamic load added by the mechanical shock and vibration requirements.

A potential mechanical solution for heavy heatsinks is the use of a supporting mechanism such as a backer plate or the utilization of a direct attachment of the heatsink to the chassis pan. In these cases, the strength of the supporting component can be utilized rather than solely relying on the baseboard strength. In addition to the previous general guidelines given, contact with the baseboard surfaces should be minimized during installation to avoid any damage to the baseboard.

Placement of board-to-chassis mounting holes also impacts board deflection and resultant socket solder ball stress. Customers need to assess the shock for their designs as heatsink retention (backplate), heatsink mass, and chassis mounting holes may vary.

§

5 Processor Thermal Management

Processor thermal management features and specifications are defined to ensure processor performance optimization within the targeted system and the processor thermal environmental conditions. It is the responsibility of the system and components thermal architects to ensure compliance with the processor thermal specifications. Compromising processor thermal requirements will impact the processor performance and reliability.

5.1 Processor Thermal Features

5.1.1 TCC Activation Temperature

The processor has a software readable field in the TEMPERATURE_TARGET register that contains the minimum temperature at which the Thermal Control Circuit (TCC) will be activated and PROCHOT_N will be asserted. The TCC activation temperature is calibrated on a part-by-part basis and normal factory variation may result in the actual TCC activation temperature being higher than the value listed in the register.

TCC activation temperatures may change based on processor stepping, frequency or manufacturing efficiencies. Consult the *Second Generation Intel® Xeon® Scalable Processors Datasheet Volume Two: Registers*, document number 338846, for more information about this register.

Use of software that reports absolute temperature could be misleading since TCC activation temperature varies from part-to-part.

5.1.2 Intel® Turbo Boost Technology

Intel® Turbo Boost Technology is a feature available on certain Second Generation Intel® Xeon® Scalable Processor SKUs that opportunistically and automatically allows the processor to run faster than the marked frequency if all of the following conditions are met:

1. Processor operating at base frequency (that is, P1 P-state)
2. Power management not active (that is, not throttling)
3. Processor operating below its temperature limit (that is, DTS < 0)
4. Processor operating below its power and current limits (that is, < TDP and <ICC_MAX). Refer to Section 5.3.2, "Fan Speed Control" for more information.

With Intel® Turbo Boost Technology enabled, the instantaneous processor power can exceed TDP for short durations resulting in increased performance.

System thermal design should consider the following important parameters (set via the BIOS).

- POWER_LIMIT_1 (PL1) = Average processor power over a long time window (default setting is TDP)

- POWER_LIMIT_2 (PL2) = Average processor power over a short time window above TDP (short excursions). Maximum allowed by the processor is 20% above TDP for all SKUs (1.2 * TDP).

Note: The actual power will include IMON inaccuracy.

- POWER_LIMIT_1_TIME (Tau) = Time constant for the exponential weighted moving average (EWMA) which optimizes performance while reducing thermal risk (dictates how quickly power decays from its peak)

Note: Although the processor can exceed PL1 (default TDP) for a certain amount of time, the Exponential Weighted Moving Average (EWMA) power will never exceed PL1.

A properly designed processor thermal solution is important to maximizing Intel® Turbo Boost Technology performance. However, heatsink performance (thermal resistance, Ψ_{CA}) is only one of several factors that can impact the amount of benefit. Other factors are the operating environment, workload, and system design. Intel® Turbo Boost Technology performance is also constrained by ICC and VCC limits. With Intel® Turbo Mode Technology enabled, the processor may run more consistently at higher power levels (but still within TDP), and be more likely at temperatures above $T_{CONTROL,}$ as compared to when Intel® Turbo Mode Technology is disabled. This may result in higher acoustics.

5.1.2.1 Designing for Turbo Performance: Intel® Turbo Boost Technology Testing

Intel® Turbo Boost Technology is a way to automatically run the processor core faster than the noted frequency. The processor must work in the power, temperature, and specification limits of the thermal design power (TDP) envelope. Single and multi-threaded application performance increase.

Availability and frequency upside of Intel® Turbo Boost Technology state depends upon a number of factors including, but not limited to, the following:

- Type of workload
- Number of active cores
- Estimated current consumption
- Estimated power consumption
- Processor temperature

When the processor is operating below these limits and the user's workload demands additional performance, the processor frequency will dynamically increase until the upper limit of frequency is reached. Intel® Turbo Boost Technology has multiple algorithms operating in parallel to manage current, power, and temperature to maximize frequency and energy efficiency.

Note: Intel® Turbo Boost Technology allows the processor to operate at a power level that is higher than its TDP configuration and data sheet specified power for short durations to maximize performance. P1 is the frequency that Intel commits to for SSE workloads at TDP. A workload such as POVRAY will eventually limit the SSE frequency below the maximum Turbo value. The AVX workloads have their own P1 frequency limits. A workload such as LINPACK* will eventually limit the AVX frequencies as well.

For Intel® Xeon® Processor Scalable Family server, the all core turbo (P0n) can be as high as seven bins above the P1 frequency. It goes even higher when some cores are turned off.

When at P0n or higher frequency, and a TDP application starts, after a very short period of time, the processor frequency will drop. There are two ways this can happen. If there are a large number of cores active, the most likely limiter will be power. If there are a medium to small number of cores active, the likelihood that temperature will be your limiter increases.

Power throttling and thermal throttling are normal behaviors for when the application load changes suddenly from low to high. Short duration thermal throttling under turbo is acceptable, and will not impact the processor end of life. Transient periods of thermal throttling when at Turbo frequencies have been observed for multiple generations.

The processor is particularly likely to thermally throttle when a small number of cores remain active as part of a cycle going from high to low to high to low to high, etc.As this is expected behavior, applications such as LINPACK* should never be used to gage the Turbo performance capability of a platform. Especially with seven bins of all core turbo and the introduction of AVX-512, these applications will cause the processor to power or thermal throttle down below the maximum turbo frequency.

Note: PL2 is 20% higher power, so DTS to Tcase delta will increase by 20%. Increased frequencies increases thermal resistance, and are usually associated with reduced core counts in operation.

5.1.3 Thermal Management

Second Generation Intel® Xeon® Scalable Processor SKUs require careful monitoring and control of temperatures on multiple silicon dies inside the package. The case temperature of multi-die SKUs is defined as the temperature measured at various locations on the surface of the Integrated Heat Spreader (IHS) above these components. Component thermal solution designers may utilize IHS power gradient at the core locations to optimize the processor cooling solution or to verify the thermal solution capability in meeting the processor thermal requirement. To allow optimal operation and long-term reliability of Intel processor-based systems, the processor must remain between the minimum and maximum case temperature (T_{CASE}) specifications as defined in the tables in the following sub-sections. Thermal solutions not designed to provide sufficient thermal cooling may affect the long-term reliability of the processor and system. Thermal profiles ensure adherence to Intel reliability requirements.

Intel assumes system boundary conditions (system ambient, airflow, heatsink performance/pressure drop, preheat, etc.) for each processor SKU. For servers, each processor will be aligned to either 1U or 2U system boundary conditions. Implementing a thermal solution that violates the thermal profile for extended periods of time may result in permanent damage to the processor or reduced life. The upper point of the thermal profile consists of the Thermal Design Power (TDP) and the corresponding T_{CASE_MAX} value (x = TDP and y = T_{CASE_MAX}) represents a thermal solution design point.

For embedded servers, communications, and storage markets, Intel has SKUs that support thermal profiles with nominal and short-term conditions designed to meet NEBS Level 3 compliance. For these SKUs, operation at either the nominal or short-term thermal profiles should result in virtually no TCC activation. Thermal profiles for these SKUs are found in this chapter as well.

Second Generation Intel® Xeon® Scalable Processors implements a methodology for managing processor temperatures that is intended to support acoustic noise reduction through fan speed control and to assure processor reliability. Selection of the

appropriate fan speed is based on the relative temperature data reported by the processor's Platform Environment Control Interface (PECI) as described in the Electrical EDS.

If the DTS value is less than $T_{CONTROL}$, then the case temperature is permitted to exceed the thermal profile, but the DTS value must remain at or below $T_{CONTROL}$.

For T_{CASE} implementations, if DTS is greater than $T_{CONTROL}$, then the case temperature must meet the T_{CASE} based thermal profiles.

For DTS implementations:

- The T_{CASE} thermal profile can be ignored during processor run time.
- If DTS is greater than $T_{CONTROL}$, then follow the DTS thermal profile specifications for fan speed optimization.

The temperature reported over PECI is always a negative value and represents a delta below the onset of Thermal Control Circuit (TCC) activation, as indicated by PROCHOT_N (see the Electrical Specification section of the EDS). Systems that implement fan speed control must be designed to use this data. Systems that do not alter the fan speed need to guarantee the case temperature meets the thermal profile specifications.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it is immeasurable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss, and in some cases may exceed the specified maximum temperature which affects the long-term reliability of the processor. In addition, a thermal solution that is significantly under-designed may not be capable of cooling the processor even when the TCC is active continuously.

(x = TDP and y = T_{CASE_MAX} @ TDP) represents a thermal solution design point. Intel recommends that complete thermal solution designs target the Thermal Design Power (TDP). The adaptive thermal monitor feature is intended to help protect the processor in the event that an application exceeds the TDP recommendation for a sustained time period. To ensure maximum flexibility for future requirements, systems should be designed to the Flexible Motherboard (FMB) guidelines, even if a processor with lower power dissipation is currently planned. The adaptive thermal monitor feature must be enabled for the processor to remain within its specifications.

5.2 Processor Thermal Specifications

The processor requires a thermal solution to maintain temperatures within operating limits. Any attempt to operate the processor outside these limits may result in permanent damage to the processor and potentially other components within the system. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete solution includes both component and system level thermal management features. Component level thermal solutions can include active or passive heatsinks attached to the processor IHS. Typical system level thermal solutions may consist of system fans combined with ducting and venting.

5.2.1 T_{CASE} and DTS Thermal Specifications

The T_{CASE} thermal based specifications are used for heatsink sizing while DTS based specifications are used for acoustic and fan speed optimizations. The Digital Thermal Sensor (DTS) reports a relative die temperature as an offset from TCC activation temperature. SKUs may share T_{CASE} thermal profiles, but they will have separate DTS based thermal profiles.

5.2.1.1 T_{CASE} Thermal Profile

For a single die processor package or non-MCP, all thermal profiles, whether based on T_{CASE} or DTS, follow the straight-line equation format namely, $y = mx + b$. Where,

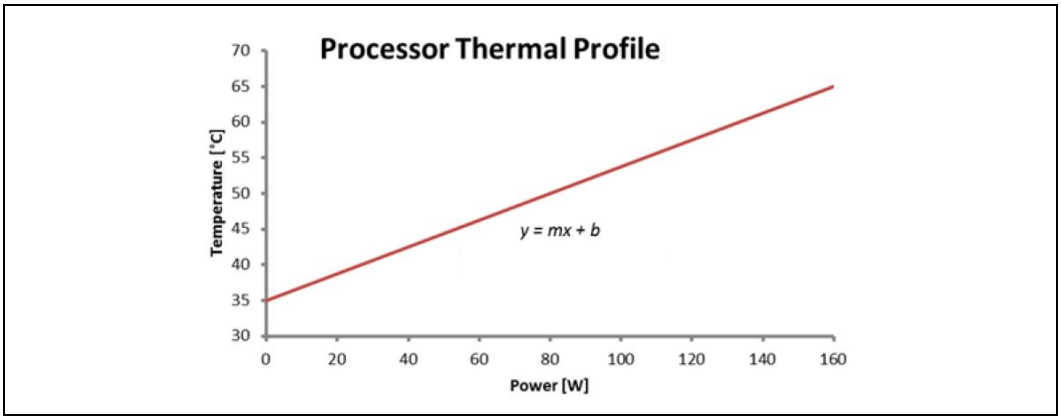
y = temperature (T) in °C

m = slope (Ψ_{CA}) (CA = Case to ambient)

x = power (P) in Watts

b = y-intercept (T_{LA}) (LA = local ambient)

Figure 5-1. Typical Thermal Profile Graph (Illustration Only)



Note: There is no one-to-one correlation between T_{CASE} and DTS. The T_{CASE} specification exists to ensure that, when the T_{CASE} margin is 0 °C, the DTS reading should be at or below DTS_Max (thermal throttle) for virtually all server processors. Variation in the DTS margin is normal and results from several factors including DTS accuracy, thermal stack up variance, actual power under a TDP load, etc. The T_{CASE} and DTS thermal profiles are expected to account for these variables.

The only way to accurately determine T_{CASE} is to measure it with a thermocouple. The T_{CASE} thermal profile specification is primarily for thermal solution sizing to ensure that virtually all processors within a particular SKU will operate with little to no thermal throttle. The DTS thermal profile provides a real time metric for FSC and acoustics, and to ensure performance and reliability. As long as a thermal solution meets the T_{CASE} thermal profile specification, it is expected to support part-to-part variation in the DTS margin.

Table 5-1. Second Generation Intel® Xeon® Scalable Processors Non-MCP SKU Thermal Specifications

Processor Brand String	TDP (W)	Core Count	Frequency (GHz)	Die	Heatsink Form Factor	System Form Factor	C1E Offset Disable[8]	$T_{CONTROL}$ (°C)	Thermal Profiles		T_{CASE_MAX} (°C)	DTS_{MAX} (°C)	Smiling Pond Correction Factor (°C/W)	Stepping	Sample Type
									T_{CASE} (°C)	DTS (°C)					
Intel® Xeon® Platinum 8280 CPU	205	28	2.7	XCC	2U	Spread Core	0	10	[0.180*P]+47	[0.263*P]+47	84	101	0	B1	Revenue
Intel® Xeon® Platinum 8270 CPU	205	26	2.7	XCC	2U	Spread Core	0	10	[0.180*P]+47	[0.278*P]+47	84	104	0	B1	Revenue
Intel® Xeon® Platinum 8268 CPU	205	24	2.9	XCC	2U	Spread Core	0	10	[0.180*P]+47	[0.278*P]+47	84	104	0	B1	Revenue
Intel® Xeon® Gold 6254 CPU	200	18	3.1	XCC	2U	Spread Core	0	10	[0.175*P]+47	[0.285*P]+47	82	104	0.001	B1	Revenue
Intel® Xeon® Gold 6246 CPU	165	12	3.3	XCC	2U	Spread Core	0	10	[0.182*P]+46	[0.321*P]+46	76	99	0.00031	B1	Revenue
Intel® Xeon® Gold 6244 CPU	150	8	3.6	XCC	2U	Spread Core	0	10	[0.187*P]+46	[0.373*P]+46	74	102	0.0025	B1	Revenue
Intel® Xeon® Platinum 8276 CPU	165	28	2.2	XCC	1U	Spread Core	0	10	[0.255*P]+47	[0.333*P]+47	89	102	-0.0011	B1	Revenue
Intel® Xeon® Platinum 8260 CPU	165	24	2.4	XCC	1U	Spread Core	0	10	[0.261*P]+47	[0.345*P]+47	90	104	0.006	B1	Revenue
Intel® Xeon® Platinum 6212U CPU	165	24	2.4	XCC	1U	Spread Core	0	10	[0.261*P]+47	[0.345*P]+47	90	104	0.006	B1	Revenue
Intel® Xeon® Platinum 6210U CPU	150	20	2.5	XCC	1U	Spread Core	0	10	[0.260*P]+47	[0.353*P]+47	86	100	0.0036	B1	Revenue
Intel® Xeon® Gold 6252 CPU	150	24	2.1	XCC	1U	Spread Core	0	10	[0.260*P]+47	[0.340*P]+47	86	98	0.0047	B1	Revenue
Intel® Xeon® Gold 6248 CPU		20	2.5	XCC	1U	Spread Core	0	10	[0.260*P]+47	[0.353*P]+47	86	100	0.0036	B1	Revenue
Intel® Xeon® Gold 6240 CPU		18	2.6	XCC	1U	Spread Core	0	10	[0.253*P]+47	[0.353*P]+47	85	100	0.0025	B1	Revenue
Intel® Xeon® Gold 6242 CPU		16	2.8	XCC	1U	Spread Core	0	10	[0.253*P]+47	[0.367*P]+47	85	102	0.002	B1	Revenue
Intel® Xeon® Gold 6234 CPU	130	8	3.3	XCC	1U	Spread Core	0	10	[0.254*P]+46	[0.415*P]+46	79	100	-0.0056	B1	Revenue
Intel® Xeon® Gold 5222 CPU	105	4	3.8	XCC	1U	Spread Core	0	10	[0.248*P]+46	[0.514*P]+46	72	100	-0.0047	B1	Revenue
Intel® Xeon® Platinum 8256 CPU			3.8	XCC	1U	Spread Core	0	10	[0.248*P]+46	[0.514*P]+46	72	100	-0.0047	B1	Revenue
Intel® Xeon® Gold 6238 CPU	140	22	2.1	XCC	1U	Spread Core	0	10	[0.250*P]+57	[0.336*P]+57	92	104	-0.0032	B1	Revenue
Intel® Xeon® Gold 6262V CPU	135	24	1.9	XCC	1U	Spread Core	0	10	[0.252*P]+57	[0.333*P]+57	91	102	0.0048	B1	Revenue
Intel® Xeon® Gold 6209U CPU	125	20	2.1	XCC	1U	Spread Core	0	10	[0.256*P]+55	[0.336*P]+55	87	97	0.0040	B1	Revenue
Intel® Xeon® Gold 6230 CPU	125	20	2.1	XCC	1U	Shadow Core	0	10	[0.256*P]+55	[0.336*P]+55	87	97	0.0040	B1	Revenue
Intel® Xeon® Gold 5220S CPU[1]		18	2.7	XCC	1U	Shadow Core	0	10	[0.256*P]+55	[0.344*P]+55	87	98	0.00142	B1	Revenue
Intel® Xeon® Gold 5218 CPU		16	2.3	XCC	1U	Shadow Core	0	10	[0.256*P]+55	[0.344*P]+55	87	98	0.0018	B1	Revenue
Intel® Xeon® Platinum 8253 CPU		16	2.2	XCC	1U	Shadow Core	0	10	[0.256*P]+55	[0.344*P]+55	87	98	0.0014	B1	Revenue
Intel® Xeon® Gold 6226 CPU	125	12	2.7	XCC	1U	Spread Core	0	10	[0.248*P]+55	[0.360*P]+55	86	100	-0.0018	B1	Revenue
Intel® Xeon® Gold 6222V CPU	115	20	1.8	XCC	1U	Spread Core	0	10	[0.252*P]+54	[0.330*P]+54	83	92	0.0035	B1	Revenue
Intel® Xeon® Gold 5217	115	8	3	HCC	1U	Spread Core	0	10	[0.287*P]+46	[0.487*P]+46	79	102	0.031	L1	Revenue

Table 5-1. Second Generation Intel® Xeon® Scalable Processors Non-MCP SKU Thermal Specifications

Processor Brand String	TDP (W)	Core Count	Frequency (GHz)	Die	Heatsink Form Factor	System Form Factor	C1E Offset Disable[8]	$T_{CONTROL}$ (°C)	Thermal Profiles		T_{CASE_MAX} (°C)	DTS_{MAX} (°C)	Smiling Pond Correction Factor (°C/W)	Stepping	Sample Type
									T_{CASE} (°C)	DTS (°C)					
Intel® Xeon® Gold 5220	125	18	2.2	HCC	1U	Shadow Core	0	10	[0.256*P]+55	[0.376*P]+55	87	102	0.005	L1	Revenue
Intel® Xeon® Gold 5218B		16	2.3	HCC	1U	Shadow Core	0	10	[0.256*P]+55	[0.376*P]+55	87	102	0.008	L1	Revenue
Intel® Xeon® Gold 5215	85	10	2.5	HCC	1U	Shadow Core	0	10	[0.282*P]+53	[0.471*P]+53	77	93	0.0281	L1	Revenue
Intel® Xeon® Silver 4216	100	16	2.1	HCC	1U	Shadow Core	0	10	[0.270*P]+52	[0.390*P]+52	79	91	0.0175	L1	Revenue
Intel® Xeon® Silver 4215	85	8	2.5	HCC	1U	Shadow Core	0	10	[0.282*P]+53	[0.435*P]+53	77	90	0.0291	L1	Revenue
Intel® Xeon® Silver 4214		12	2.2	HCC	1U	Shadow Core	0	10	[0.282*P]+53	[0.412*P]+53	77	88	0.0266	L1	Revenue
Intel® Xeon® Silver 4210	85	10	2.2	LCC	1U	Shadow Core	0	10	[0.282*P]+54	[0.424*P]+54	78	90	0.0429	R1	Revenue
Intel® Xeon® Silver 4208		8	2.1	LCC	1U	Shadow Core	0	10	[0.282*P]+54	[0.424*P]+54	78	90	0.0397	R1	Revenue
Intel® Xeon® Bronze 3204		6	1.9	LCC	1U	Shadow Core	0	10	[0.282*P]+53	[0.435*P]+53	77	90	0.0343	R1	Revenue

Notes:

1. Second Generation Intel® Xeon® Scalable Processors Gold –N and –S processors have been optimized for use in some networking and storage applications. The workload (TDP) assumed for maintaining the marked frequency (also called P1) is an average across the SPECint_rate2006 benchmark suite. Note that the SPECint_rate2006 benchmark is composed of 12 different sub-benchmarks. Second Generation Intel® Xeon® Scalable Processors Gold –N and –S processors assume a less intensive core workload for the TDP operating point.

   This new family of application optimized SKUs may not maintain their marked frequency while running some standard server workloads (SPECint*, SPECfp*, or POVRAY* for example). Throttling can occur even if there is thermal margin to T_{CASE_MAX} as TDP is enforced by the Power Control Unit (PCU).

   Intel recommends potential customers do performance testing using existing platforms before committing to a design using these new processors and avoid relying on previous experience and frequency scaling projections to estimate expected performance.

Table 5-2. Second Generation Intel® Xeon® Scalable Processors High Frequency Thermal Specifications

Processor Brand String	TDP (W)	Core Count	Frequency (GHz)	Die	Heatsink Form Factor	System Form Factor	C1E Offset Disable[8]	$T_{CONTROL}$ (°C)	Thermal Profiles		T_{CASE_MAX} (°C)	DTS_{MAX} (°C)	Smiling Pond Correction Factor (°C/W)	Stepping	Sample Type
									T_{CASE} (°C)	DTS (°C)					
Intel® Xeon® Gold 6256	205	12	3.6	XCC	Unique	Unique	0	10	[0.132*P]+37	[0.283*P]+37	64	95	0.0016	B1	Revenue
Intel® Xeon® Gold 6250	185	8	3.9	XCC	Unique	Unique	0	10	[0.124*P]+37	[0.314*P]+37	60	95	0.0075	B1	Revenue

Table 5-3. Second Generation Intel® Xeon® Scalable Processors Refresh Non-MCP SKU Thermal Specifications

Processor Brand String	TDP (W)	Core Count	Frequency (GHz)	Die	Heatsink Form Factor	System Form Factor	C1E Offset Disable[8]	$T_{CONTROL}$ (°C)	Thermal Profiles		T_{CASE_MAX} (°C)	$DTS_{\_MAX}$ (°C)	Smiling Pond Correction Factor (°C/W)	Stepping	Sample Type
									T_{CASE} (°C)	DTS (°C)					
Intel® Xeon® Platinum 8279W CPU	205	28	2.5	XCC	WS	2S-WS	0	10	[0.166*P]+42	[0.249*P]+42	76	93	-0.001	B1	Revenue
Intel® Xeon® Platinum 8267W CPU	205	24	2.7	XCC	WS	2S-WS	0	10	[0.176*P]+42	[0.268*P]+42	78	97	0.008	B1	Revenue
Intel® Xeon® Gold 6253W	200	18	3.1	XCC	WS	2S-WS	0	10	[0.170*P]+42	[0.280*P]+42	76	98	0.001	B1	Revenue
Intel® Xeon® Gold 6245W	180	12	3.3	XCC	WS	2S-WS	0	10	[0.167*P]+42	[0.306*P]+42	72	97	0.002	B1	Revenue
Intel® Xeon® Gold 6241W	205	16	3.2	XCC	WS	2S-WS	0	10	[0.171*P]+42	[0.288*P]+42	77	101	0.004	B1	Revenue
Intel® Xeon® Gold 6233W	160	8	3.8	XCC	WS	2S-WS	0	10	[0.169*P]+41	[0.369*P]+41	68	100	0.001	B1	Revenue
Intel® Xeon® Gold 5216W	160	8	3.5	XCC	WS	2S-WS	0	10	[0.169*P]+41	[0.350*P]+41	68	97	0.000	B1	Revenue
Intel® Xeon® Gold 6258R	205	28	2.7	XCC	2U	Spread Core Extended Air	0	10	[0.161*P]+41	[0.244*P]+41	74	91	0.000	B1	Revenue
Intel® Xeon® Gold 6248R	205	24	3	XCC	2U	Spread Core Extended Air	0	10	[0.166*P]+41	[0.263*P]+41	75	95	0.003	B1	Revenue
Intel® Xeon® Gold 6242R	205	20	3.1	XCC	2U	Spread Core Extended Air	0	10	[0.171*P]+41	[0.273*P]+41	76	97	0.0075	B1	Revenue
Intel® Xeon® Gold 6246R	205	16	3.4	XCC	2U	Spread Core Extended Air	0	10	[0.166*P]+41	[0.293*P]+41	75	101	0.0044	B1	Revenue
Intel® Xeon® Gold 6238R	165	28	2.2	XCC	1U	Spread Core	0	10	[0.255*P]+47	[0.333*P]+47	89	102	-0.0011	B1	Revenue
Intel® Xeon® Gold 6240R	165	24	2.4	XCC	1U	Spread Core	0	10	[0.261*P]+47	[0.345*P]+47	90	104	0.006	B1	Revenue
Intel® Xeon® Gold 6230R	150	26	2.1	XCC	1U	Spread Core	0	10	[0.253*P]+47	[0.333*P]+47	85	97	-0.001	B1	Revenue
Intel® Xeon® Gold 5220R	150	24	2.2	XCC	1U	Spread Core	0	10	[0.260*P]+47	[0.340*P]+47	86	98	0.0047	B1	Revenue
Intel® Xeon® Gold 6226R	150	16	2.9	XCC	1U	Spread Core	0	10	[0.253*P]+47	[0.367*P]+47	85	102	0.002	B1	Revenue
Intel® Xeon® Gold 6208U	150	16	2.9	XCC	1U	Spread Core	0	10	[0.253*P]+47	[0.367*P]+47	85	102	0.002	B1	Revenue
Intel® Xeon® Gold 4215R	130	8	3.2	XCC	1U	Spread Core	0	10	[0.254*P]+46	[0.415*P]+46	79	100	-0.0056	B1	Revenue
Intel® Xeon® Gold 5218R	125	20	2.1	XCC	1U	Shadow Core	0	10	[0.256*P]+55	[0.336*P]+55	87	97	0.004	B1	Revenue
Intel® Xeon® Gold 5220R	125	18	2.2	HCC	1U	Shadow Core	0	10	[0.256*P]+55	[0.376*P]+55	87	102	0.005	L1	Revenue
Intel® Xeon® Gold 5218R		16	2.3	HCC	1U	Shadow Core	0	10	[0.256*P]+55	[0.376*P]+55	87	102	0.008	L1	Revenue
Intel® Xeon® Gold 5215R	100	10	2.7	HCC	1U	Shadow Core	0	10	[0.280*P]+52	[0.470*P]+52	80	99	0.0281	L1	Revenue
Intel® Xeon® Silver 4216R	125	16	2.3	HCC	1U	Shadow Core	0	10	[0.256*P]+55	[0.376*P]+55	87	102	0.008	L1	Revenue

Table 5-3. Second Generation Intel® Xeon® Scalable Processors Refresh Non-MCP SKU Thermal Specifications

Processor Brand String	TDP (W)	Core Count	Frequency (GHz)	Die	Heatsink Form Factor	System Form Factor	C1E Offset Disable[8]	$T_{CONTROL}$ (°C)	Thermal Profiles		T_{CASE_MAX} (°C)	DTS_{MAX} (°C)	Smiling Pond Correction Factor (°C/W)	Stepping	Sample Type
									T_{CASE} (°C)	DTS (°C)					
Intel® Xeon® Silver 4214R	100	12	2.5	HCC	1U	Shadow Core	0	10	[0.270*P]+52	[0.420*P]+52	79	94	0.0266	L1	Revenue
Intel® Xeon® Gold 4213W	115	16	3.0	HCC	1U	Spread Core	0	10	[0.256*P]+55	[0.376*P]+55	84	98	0.031	L1	Revenue
Intel® Xeon® Gold 5219W	125	18	2.2	HCC	1U	Shadow Core	0	10	[0.256*P]+55	[0.376*P]+55	87	102	0.005	L1	Revenue
Intel® Xeon® Gold 5214W	125	16	2.3	HCC	1U	Shadow Core	0	10	[0.256*P]+55	[0.376*P]+55	87	102	0.008	L1	Revenue
Intel® Xeon® Gold 5213W	100	10	2.7	HCC	1U	Shadow Core	0	10	[0.280*P]+52	[0.470*P]+52	80	99	0.0281	L1	Revenue
Intel® Xeon® Gold 4211W	100	12	2.5	HCC	1U	Shadow Core	0	10	[0.270*P]+52	[0.420*P]+52	79	94	0.0266	L1	Revenue
Intel® Xeon® Silver 4210R	100	10	2.5	LCC	1U	Shadow Core	0	10	[0.280*P]+56	[0.420*P]+56	84	98	0.0429	R1	Revenue
Intel® Xeon® Silver 4208R	100	8	2.3	LCC	1U	Shadow Core	0	10	[0.280*P]+56	[0.430*P]+56	84	99	0.0408	R1	Revenue
Intel® Xeon® Bronze 3206R	85	8	2.1	LCC	1U	Shadow Core	0	10	[0.282*P]+54	[0.424*P]+54	78	90	0.0397	R1	Revenue

5.2.2 Intel® Speed Select Technology (Intel® SST) on Second Generation Intel® Xeon® Scalable Processors

Intel® Speed Select Technology (Intel® SST) is a feature that provides flexibility and configurability of the desired base performance. It has the capability to configure the CPU to run at three distinct operating points:

- Each operating point defined by a combination of core count/base frequency/TDP/T_j

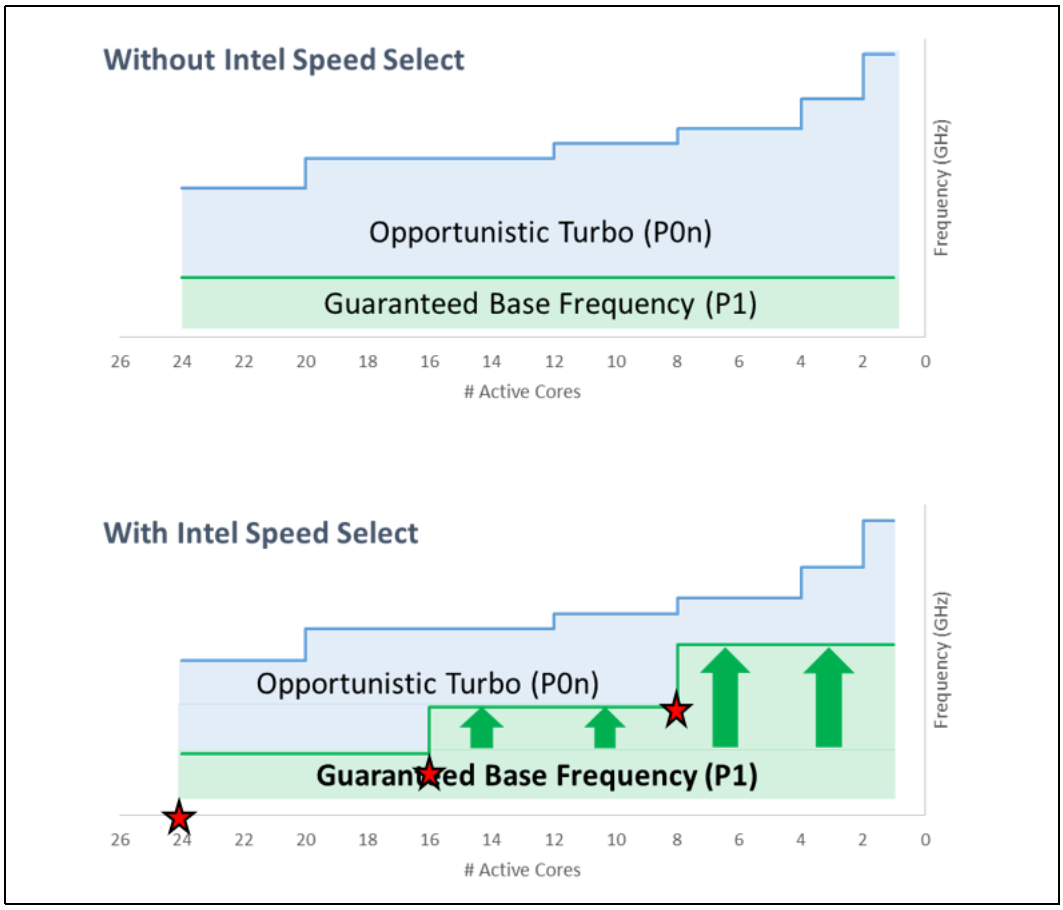
Static Boot Time Configuration:

- The BIOS discovers and configures the operating point at boot.

Key Value Prop:

- Multiple CPU personalities based on workload/VM needs
- Improved server utilization in data center
- Improved guaranteed performance SLAs

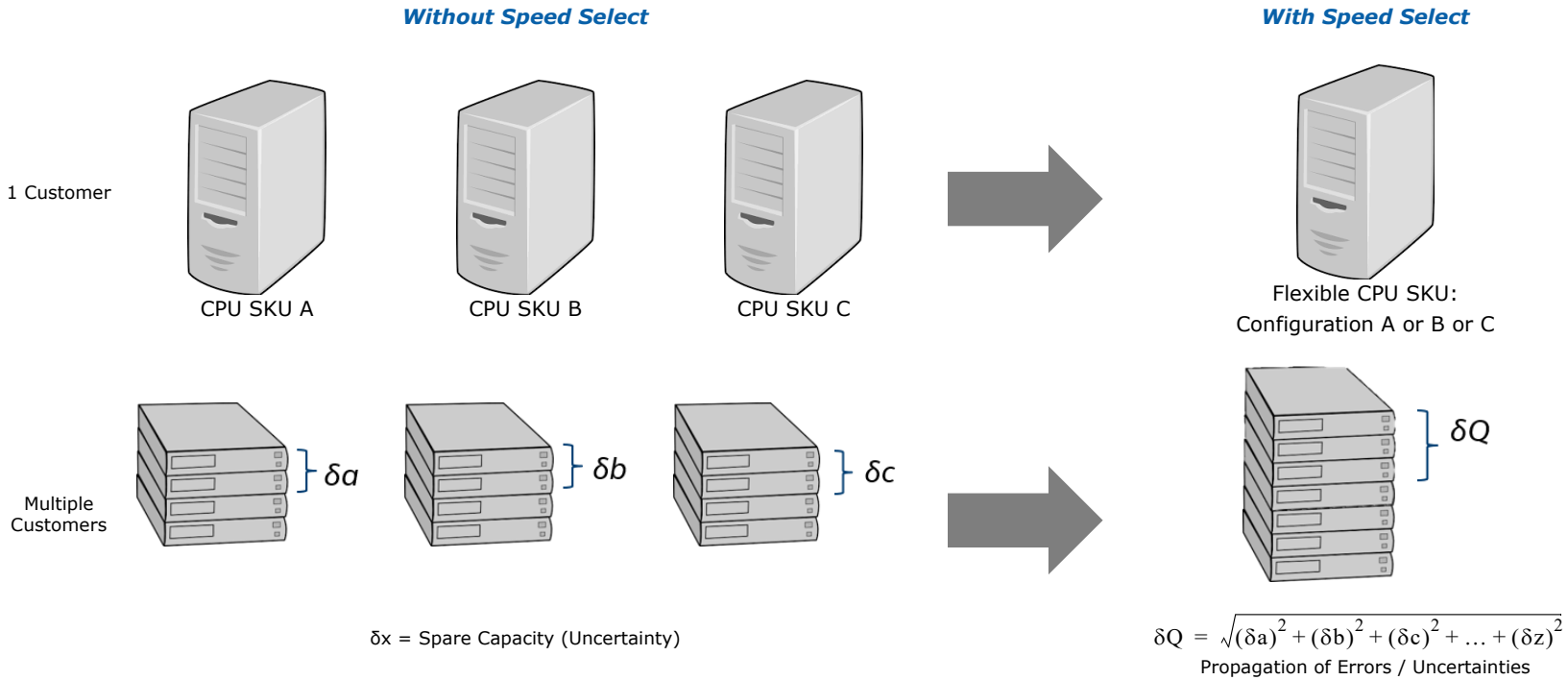
Figure 5-2. Intel® Speed Select Technology (Intel® ISS)



Note: Frequency and core count for illustration only.

5.2.2.1 Benefits of Flexible CPU Configuration - Example

- Cloud customer has three distinct products with different hardware configurations.
- Targets 50%+ utilization to accommodate fluctuations in demand/uncertainty on customer product choice.
- By consolidating three hardware configurations to single flexible SKU, the CSP can reduce the total number of system deployments and still meet the same demand/uncertainty profile.



5.2.2.2 Thermal and Fan Speed Control Considerations

DTS 2.0 is not available in Intel® Speed Select Technology configurations.

- DTS 2.0 thermal "Margin to Loadline" is available only for the base configuration.
- Same margin sensor reports "Margin to Tcontrol" for ISS configurations for fan speed control.

System power characterization must be done for all configurations as fan behavior might change among configurations.

"Margin to Throttle" is available on all configurations (Base and ISS configurations).

Figure 5-3. Examples of DTS 2.0 Based Thermal Margin on Base and ISS Configurations

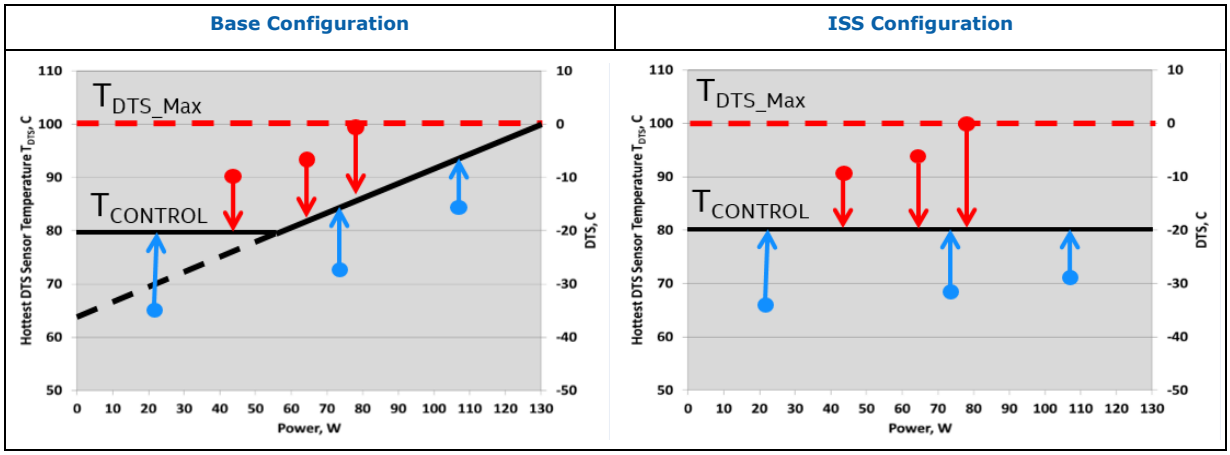


Table 5-4. Second Generation Intel® Xeon® Scalable Processors - SP ISS Thermal Specifications

Processor Number	Configuration	TDP (W)	Core Count	Frequency (GHz)	Die	Heatsink Form Factor	System Form Factor	C1E Offset Disable[8]	$T_{CONTROL}$ (°C)	Thermal Profiles		T_{CASE_MAX} (°C)	DTS_{MAX} (°C)	Smiling Pond Correction Factor (°C/W)	Stepping	Sample Type
										T_{CASE} (°C)	DTS (°C)					
Intel® Xeon® Gold 6240Y	Baseline	150	18	2.6	XCC	2U	Spread Core	0	5	[0.187*P]+46	[0.280*P]+46	74	88	0.0026	B1	Revenue
	ISS0	150	14	2.8	XCC		Spread Core	0	5	[0.187*P]+46	No DTS 2.0 Thermal Profile[1]	74	Note 1	0.0058		
	ISS1	150	8	3.1	XCC		Spread Core	0	5	[0.180*P]+46		73		-0.0012		
Intel® Xeon® Gold 6252N[3]	Baseline	150	24	2.3	XCC	2U	Spread Core	0	10	[0.187*P]+46	[0.267*P]+46	74	86	0.0057	B1	Revenue
	PBF	150	8	2.8	XCC		Spread Core	0	10	[0.187*P]+46	No DTS 2.0 Thermal Profile[1]	74	Note 1			
			16	2.1	XCC		Spread Core									
Intel® Xeon® Platinum 8260Y	Baseline	165	24	2.4	XCC	1U	Spread Core	0	7	[0.261*P]+47	[0.345*P]+47	90	104	0.006	B1	Revenue
	ISS0	155	20	2.5	XCC		Spread Core	0	7	[0.258*P]+47	No DTS 2.0 Thermal Profile[1]	87	Note 1	0.0036		
	ISS1	150	16	2.7	XCC		Spread Core	0	7	[0.253*P]+47		85		0.002		
Intel® Xeon® Gold 6230N[3]	Baseline	125	20	2.3	XCC	1U	Spread Core	0	10	[0.256*P]+46	[0.344*P]+46	78	89	0.004	B1	Revenue
	PBF	125	6	2.7	XCC		Spread Core	0	10	[0.256*P]+46	No DTS 2.0 Thermal Profile[1]	78	Note 1			
			14	2.1	XCC		Spread Core									
Intel® Xeon® Silver 4214Y	Baseline	85	12	2.2	HCC	1U	Shadowed	0	5	[0.282*P]+53	[0.412*P]+53	77	88	0.0332	L1	Revenue
	ISS0	85	10	2.3	HCC	1U	Shadowed	0	5	[0.282*P]+53	No DTS 2.0 Thermal Profile[1]	77	Note 1	0.0285		
	ISS1	85	8	2.4	HCC	1U	Shadowed	0	5	[0.282*P]+53		77		0.0291		
Intel® Xeon® Gold 5218N[3]	Baseline	110	16	2.3	HCC	1U	Shadowed	0	10	[0.273*P]+53	[0.373*P]+53	83	94	0.018	L1	Revenue
	PBF	110	4	2.7	HCC	1U	Shadowed	0	10	[0.273*P]+53	No DTS 2.0 Thermal Profile[1]	83	Note 1	0.022		
			12	2.1	HCC	1U	Shadowed	0	10							

Notes:

1. Used $T_{Control}$ specification.
2. For these ISS SKUs, DTS 2.0 is supported only for the baseline configuration. For ISS and PBF configurations, DTS 2.0 is not supported. The sensor that reports margin to DTS 2.0 thermal profile will report margin to $T_{Control}$ for fan speed control purposes.
3. Second Generation Intel® Xeon® Scalable Processors Gold –N and –S processors have been optimized for use in some networking and storage applications. The workload (TDP) assumed for maintaining the marked frequency (also called P1) is an average across the SPECint_rate2006 benchmark suite. Note that the SPECint_rate2006 benchmark is composed of 12 different sub-benchmarks. Second Generation Intel® Xeon® Scalable Processors Gold –N and –S processors assume a less intensive core workload for the TDP operating point.
   This new family of application optimized SKUs may not maintain their marked frequency while running some standard server workloads (SPECint*, SPECfp*, or POVRAY* for example). Throttling can occur even if there is thermal margin to T_{CASE_MAX} as TDP is enforced by the Power Control Unit (PCU).
   Intel recommends potential customers do performance testing using existing platforms before committing to a design using these new processors and avoid relying on previous experience and frequency scaling projections to estimate expected performance.

5.2.2.3 Non-MCP (10-Year Use + NEBS-Friendly) SKU Thermal Profiles

Network Equipment Building System (NEBS) is the most common set of environmental design guidelines applied to telecommunications equipment. Non-MCP (10-year use + NEBS-friendly) SKU thermal profiles target operation at higher case temperatures and/or NEBS thermal profiles for embedded communications server and storage form factors. The term “embedded” is used to refer to those segments collectively. Thermal profiles in this section pertain only to those specific non-MCP (10-year use + NEBS-friendly) SKU thermal profiles.

The nominal thermal profile must be used for standard operating conditions or for products that do not require NEBS Level 3 compliance.

The short-term thermal profile may only be used for short-term excursions to higher ambient operating temperatures, not to exceed 96 hours per instance, 360 hours per year, and a maximum of 15 instances per year, as intended by NEBS Level 3.

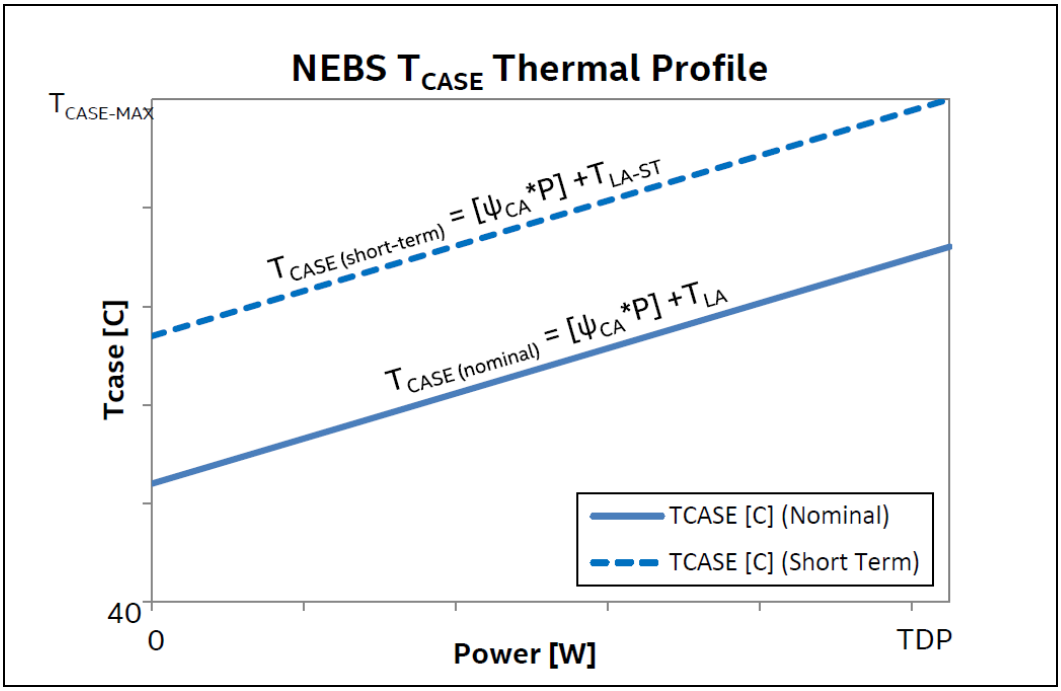
Operation at the short-term thermal profile for durations exceeding 360 hours per year violate the processor thermal specifications and may result in permanent damage to the processor.

Implementation of the defined thermal profile should result in virtually no TCC activation.

5.2.2.4 NEBS T_{CASE} Thermal Profile

The NEBS thermal profiles help relieve thermal constraints for short-term NEBS conditions. To help with reliability, the processors must meet the nominal thermal profile under standard operating conditions and can only rise up to the short-term specification for the NEBS excursions. See the following thermal profile diagram.

Figure 5-4. NEBS Thermal Profile



Notes:
1. The nominal thermal profile must be used for all normal operating conditions, or for products that do not require NEBS Level 3 compliance.
2. The short-term thermal profile may only be used for short-term excursions to higher ambient operating temperatures, not to exceed 360 hours per year as compliant with NEBS Level 3.
3. Implementation of either thermal profile should result in virtually no TCC activation. Utilization of a thermal solution that exceeds the short-term thermal profile, or which operates at the short-term thermal profile for a duration longer than the limits specified in Note 2, do not meet the processor thermal specifications and may result in permanent damage to the processor.

5.2.2.5 NEBS T_{DTS} Thermal Profile

The thermal solution is expected to be developed in accordance with the T_{CASE} thermal profile. Operational compliance monitoring of thermal specifications and fan speed modulation may be done via the DTS based thermal profile.

These T_{DTS} profiles are fully defined by the simple linear equation: $T_{DTS} = PSI_{PA} * P + T_{LA}$

Where:

PSI_{PA} is the processor-to-ambient thermal resistance of the processor thermal solution.

T_{LA} is the local ambient temperature for the nominal thermal profile.

T_{LA-ST} designates the local ambient temperature for short-term operation.

P is the processor power dissipation.

Figure 5-5 illustrates the general form of the resulting linear graph resulting from $T_{DTS} = PSI_{PA} * P + T_{LA}$.

The slope of a DTS profile assumes full fan speed which is not required over much of the power range. $T_{CONTROL}$ is the temperature above that fans must be at maximum speed to meet the thermal profile requirements. $T_{CONTROL}$ is different for each SKU and

may be slightly above or below $T_{DTS-Max}$ of the DTS nominal thermal profile for a particular SKU. At many power levels on most non-MCP (10-year use + NEBS-friendly) SKU thermal profiles, temperatures of the nominal profile are less than $T_{CONTROL}$ as indicated by the blue shaded region in the DTS thermal profile in the following diagram. As a further simplification, operation at DTS temperatures up to $T_{CONTROL}$ is permitted at all power levels. Compliance to the DTS profile is required for any temperatures exceeding $T_{CONTROL}$.

Figure 5-5. NEBS DTS Thermal Profile

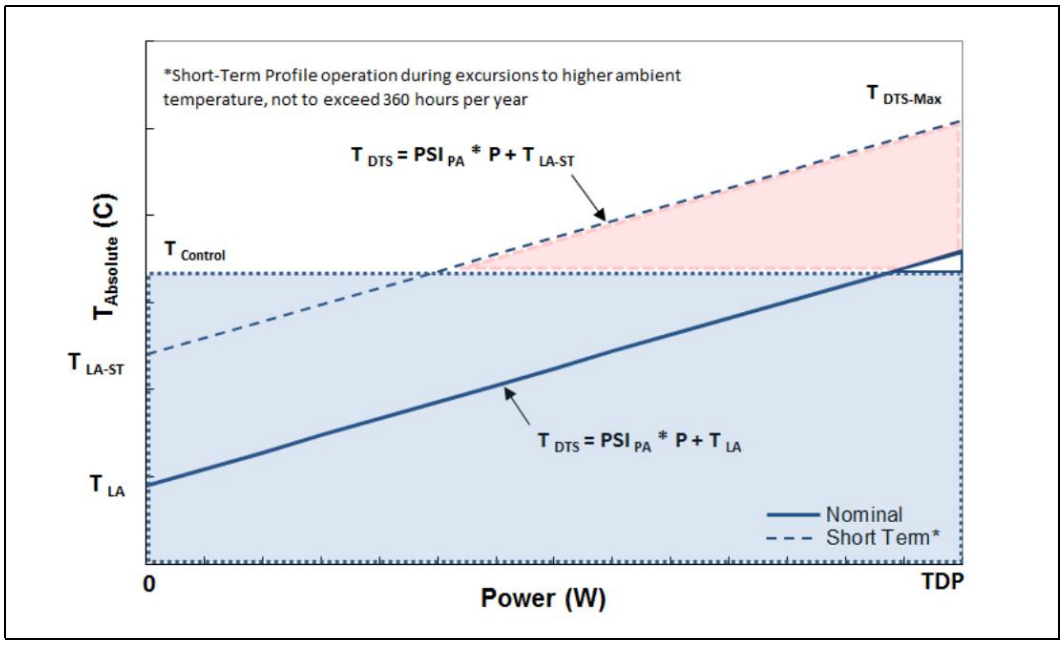
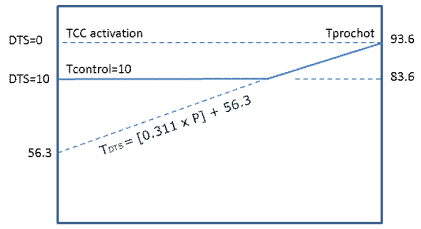
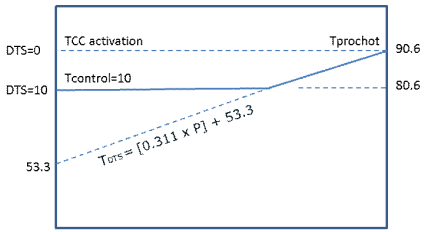


Table 5-5. Second Generation Intel® Xeon® Scalable Processors-SP_HT XCC Thermal Specs Update

Processor Number	TDP (W)	Die	Frequency (GHz)	Core Count	C1E Offset Disable[8]	$T_{CONTROL}$	Thermal Profiles				Short Term T_{CASE_MAX}	Short Term $DTS_{\_MAX}$ (°C)	Nominal T_{CASE_MAX}	Nominal $DTS_{\_MAX}$ (°C)	Correction Factor (°C/W)	Stepping	Sample Type
							Nominal T_{CASE_MAX} (°C)	Short Term T_{CASE_MAX} (°C)	Nominal $DTS_{\_MAX}$ (°C)	Short Term $DTS_{\_MAX}$ (°C)							
Intel® Xeon® Gold 6238T	125	XCC	1.9	22	0	20	[0.208*P]+52	[0.208*P]+67	[0.296*P]+52	[0.296*P]+67	93	104	78	89	0.0063	B1	Revenue
Intel® Xeon® Gold 6230T	125	XCC	2.1	20	0	20	[0.200*P]+52	[0.200*P]+67	[0.280*P]+52	[0.280*P]+67	92	102	77	87	0.004	B1	Revenue
Intel® Xeon® Gold 5220T	105	XCC	1.9	18	0	20	[0.248*P]+52	[0.248*P]+67	[0.333*P]+52	[0.333*P]+67	93	102	78	87	-0.0039	B1	Revenue
Intel® Xeon® Gold 5218T	105	XCC	2.1	16	0	20	[0.248*P]+52	[0.248*P]+67	[0.333*P]+52	[0.333*P]+67	93	102	78	87	0.0071	B1	Revenue
Intel® Xeon® Gold 4209T	70	LCC	2.2	8	0	20	[0.343*P]+52	[0.343*P]+67	[0.500*P]+52	[0.500*P]+67	91	102	76	87	0.04	R1	Revenue
Intel® Xeon® Silver 4210T	95	LCC	2.3	10	0	20	[0.253*P]+52	[0.253*P]+67	[0.368*P]+52	[0.368*P]+67	91	102	76	87	0.0434	R1	Revenue

Notes:

1. These values are specified at VccIN_MAX for all processor frequencies. Systems must be designed to ensure the processor is not subjected to any static Vcc and Icc combination wherein VccIN exceeds VccIN_MAX at a specified Icc. Refer to the electrical loadline specifications.
2. Thermal Design Power (TDP) should be used as a target for processor thermal solution design at maximum T_{CASE}. Processor power may exceed TDP for short durations.
3. These specifications are preliminary and will be updated as further characterization data becomes available.
4. Thermal specifications are based on a 12C rise above system ambient.
5. The nominal thermal profile must be used for all normal operating conditions or for products that do not require NEBS Level 3 compliance.
6. The short-term thermal profile may only be used for short-term excursions to higher ambient operating temperatures, not to exceed 96 hours per instance, 360 hours per year, and a maximum of 15 instances per year, as compliant with NEBS Level 3. Operation at the short-term thermal profile for durations exceeding 360 hours per year violate the processor thermal specifications and may result in permanent damage to the processor.
7. The DTS2.0 does follow the nominal DTS thermal profile.
8. Disabling C1E will result in an automatic reduction of DTS_max so that the reliability is still protected. DTS_max will be reduced by the value shown "C1E Offset Disable". If thermal design has not been optimized to the reduced DTS_max value, throttling may occur. $T_{CONTROL}$ is already an offset to DTS_max; therefore, the absolute temperature at which the $T_{CONTROL}$ is reached will shift by the same amount. For example:

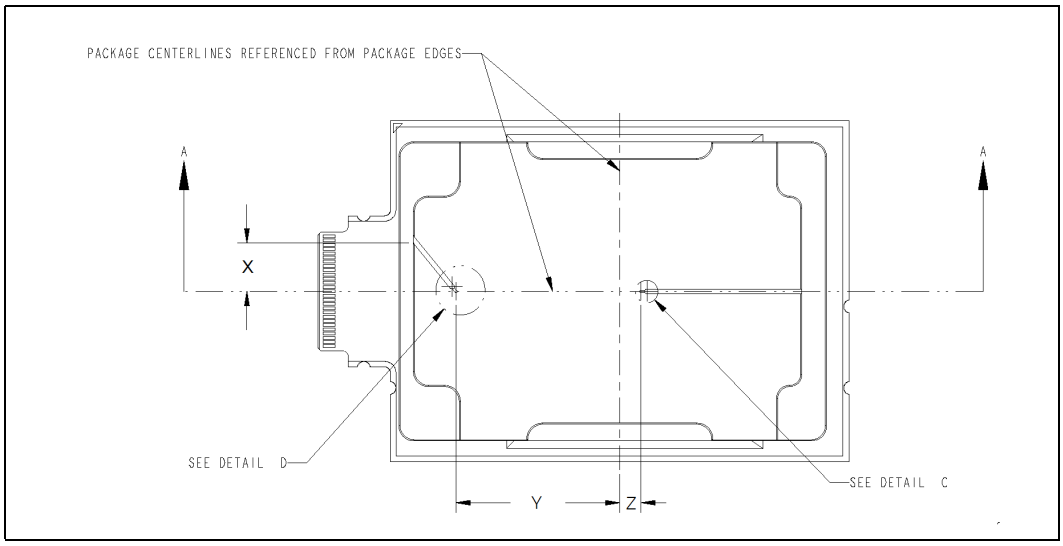
Thermtrip_abs C1E enabled = Thermtrip_abs C1E disabled	Thermtrip_abs C1E enabled = Thermtrip_abs C1E disabled
	
C1E enabled	C1E disabled

5.2.3 Thermal Metrology

5.2.3.1 Case Temperature Measurement

Processor die(s) may be off center under the Integrated Heat Spreader (IHS). The minimum and maximum case temperatures (T_{CASE}) specified are measured on the topside of the IHS, where the center of the each die is located as shown in Figure 5-6. This figure also includes geometry guidance for modifying the IHS to accept a thermocouple probe.

Figure 5-6. Case Temperature (T_{CASE}) Measurement Location



Note: Image shown here is for demonstration purposes and does not reflect final product. Refer to the mechanical drawings section for an accurate representation.

5.2.3.2 DTS 2.0 Based Thermal Margin

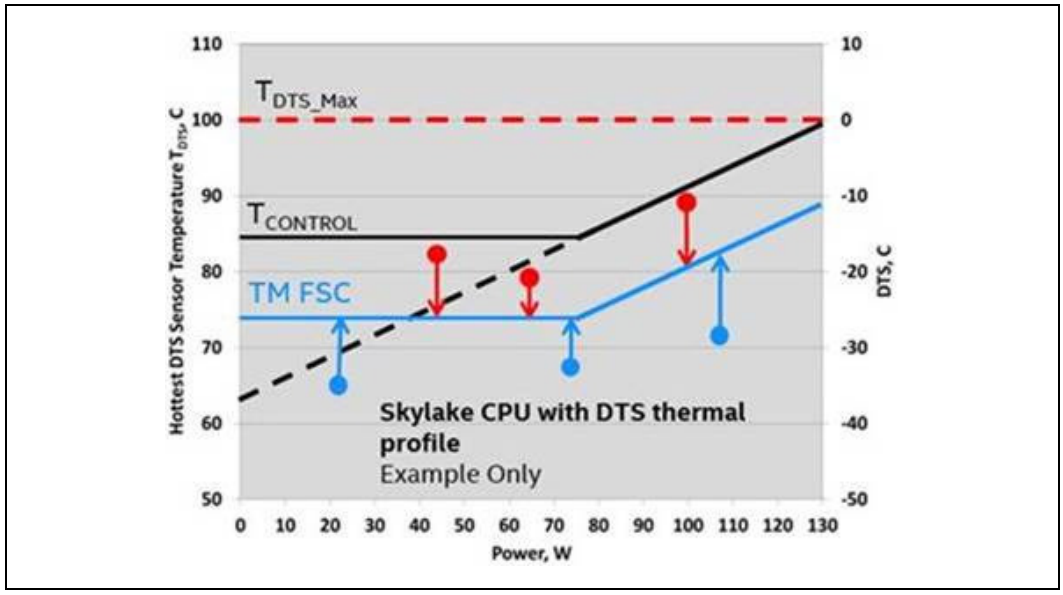
Processors covered in this document support DTS 2.0 based thermal margin. The intercept and slope terms from the DTS thermal profiles are stored in the processor. The processor calculates and reports the margin which may be read by PECI command RdPkgConfig(), Index 10; Or MSR 1A1h: PACKAGE_THERM_MARGIN[15:0]. Fan speed control algorithms simply read and react to the thermal margin register. The thermal margin offset may need to be used for real-time thermal specification compliance and power performance optimization during fan speed control. Larger thermal margin offset leads to more performance. Small thermal margin offset leads to lower fan speed and noise. The CPU package temperature is not allowed to exceed the DTS2.0 thermal specification all the time during fan speed control in normal system operating condition, which means thermal margin (MSR 1A1h) should maintain positive values all the time.

Note: The default value reported for DTS 2.0 thermal margin during bring up is 0, and this value may continue until the system is fully operational

Thermal Margin FSC = Thermal Margin (by PECI/MSR) – Thermal Margin Offset

Thermal Margin FSC < 0: Gap to thermal margin FSC specification, fan speed must increase
Thermal Margin FSC > 0: Margin to thermal margin FSC specification, fan speed may decrease

Figure 5-7. Thermal Margin to FSC Specification on Second Generation Intel® Xeon® Scalable Processors (Non-MCP)



5.3 Processor Thermal Management Guidelines

5.3.1 Processor Thermal Solution Environmental Conditions

Processor heatsink design must comply with the T_{CASE} based thermal profile. Systems that do not monitor the processor die temperature by monitoring the thermal sensor output must ensure processor cooling solution is capable of meeting the processor based T_{CASE} specification. In some situations, implementation of DTS based thermal specification can reduce average fan power and improve acoustics as compared to the T_{CASE} based thermal profile.

When all cores are active, a properly sized heatsink will be able to meet the processor thermal specification. When all cores are not active or when Intel® Turbo Boost Technology is active, attempting to comply with the DTS based thermal specification may drive system fans to increased speed. In such situations, the T_{CASE} temperature will be below the T_{CASE} based thermal profile by design.

Table 5-6 provides thermal boundary conditions and performance targets applied in defining the processor thermal specifications. These values serve as a guide for designing a process compatible thermal solution.

Table 5-6. Thermal Boundary Conditions

Heatsink Form Factor	Driving Form Factor	Thermal Specification Setting SKU Alignment	Airflow (CFM)	Boundary Conditions[1]														
				T_{LA} for each TDP SKU (°C) ($T_{SYSTEM\_AMBIENT}$ = 35 °C)														
				45 (W)	55 (W)	65 (W)	85 (W)	105 (W)	115 (W)	125 (W)	140 (W)	150 (W)	165 (W)	175 (W)	185 (W)	195 (W)	200 (W)	205 (W)
1U High Performance	½ Width	SKUs ≤ 95W	11.6	47.1	48.2	49.2	51.3	--	--	--	--	--	--	--	--	--	--	--
1U High Performance	½ Width	95W ≤ SKUs ≤ 140W	11.6	--	--	--	--	50.1	51.2	52.2	53.8	--	--	--	--	--	--	--
1U Low Impedance	½ Width	SKUs ≤ 140W	11.6	40	40	40	40	40	40	40	40	--	--	--	--	--	--	--
1U High Performance	Spread-Core 1U Height	150W ≤ SKUs ≤ 165W	11.1	--	--	--	--	--	--	--	--	43.2	43.2	--	--	--	--	--
2U Passive High Performance	2U EEB or ½ Width 2U Height	150W ≤ SKUs ≤ 165W	21.5	--	--	--	--	--	--	--	--	54.1	55.9	--	--	--	--	--
1U High Performance	Spread-Core 1U Height	High Frequency SKUs ≤ 150W Only	11.1	43.2	43.2	43.2	43.2	43.2	43.2	43.2	43.2	43.2	--	--	--	--	--	--
2U Passive High Performance	Spread-Core 2U Height	High Frequency SKUs ≤ 165W Only	21.5	43.2	43.2	43.2	43.2	43.2	43.2	43.2	43.2	43.2	43.2	--	--	--	--	--
Workstation Tower Square Passive	Workstation	Workstation SKU Only	23.5	--	--	--	--	--	--	--	--	--	41.3	--	--	--	--	--
2U Passive High Performance	Spread-Core 2U Height	175W ≤ SKUs ≤ 205W	21.5	--	--	--	--	--	--	--	--	--	--	43.2	43.2	43.2	43.2	43.2

Notes:
1. Thermal Boundary Conditions (BC) based on test data
2. 1U narrow high performance HS is used for the rear CPU, and low impedance 1U narrow HS is used for the front CPU.
3. 1U low impedance heatsink intended to use for front processor of ½ width form factor

5.3.2 Fan Speed Control

Fan Speed Control (FSC) techniques to reduce system-level acoustic noise are a common practice in server designs. The fan speed is one of the parameters that determines the amount of airflow provided to the thermal solution. Additionally, airflow is proportional to a thermal solution's performance, which consequently determines the T_{CASE} of the processor at a given power level. Because the temperature of a processor is an important parameter in determining the long-term reliability of a processor, the FSC implemented in a system directly correlates to the processor's ability to meet the thermal profile. For this purpose, the parameter called $T_{CONTROL}$, as explained in the EDS electrical specification, is to be used in FSC designs to ensure that the long-term reliability of the processor is met while keeping the system-level acoustic noise down.

When Digital Temperature Sensor (DTS) value is less than $T_{CONTROL}$, the thermal profile can be ignored. The DTS value is a relative temperature to PROCHOT which is the maximum allowable temperature before the thermal control circuit is activated. In this region, the DTS value can be utilized to not only ensure specification compliance but also to optimize fan speed control resulting in the lowest possible fan power and acoustics under any operating conditions. When DTS goes above $T_{CONTROL}$, fan speed must increase to bring the sensor temperature below $T_{CONTROL}$ or to ensure compliance with the thermal profile.

Condition	FSC Scheme
DTS<= $T_{CONTROL}$	FSC can adjust fan speed to maintain DTS ≤ $T_{CONTROL}$ (low acoustic region).
DTS > $T_{CONTROL}$	FSC should adjust fan speed to keep T_{CASE} at or below the thermal profile specification (increased acoustic region).

The PECI temperature reading from the processor can be compared to this $T_{CONTROL}$ value. A fan speed control scheme can be implemented as described in the EDS electrical specification without compromising the long-term reliability of the processor.

The PECI command for DTS is GetTemp(). Though use of a sign bit, the value returned from PECI is negative.

The PECI command for $T_{CONTROL}$ is RdPkgConfig(), temperature target read, 15:8. The value returned from PECI is unsigned (positive); however, it is negative by definition.

There are many different ways of implementing fan speed control, including FSC based on processor ambient temperature, FSC based on processor Digital Thermal Sensor (DTS) temperature, or a combination of the two. If FSC is based only on the processor ambient temperature, low acoustic targets can be achieved under low ambient temperature conditions. However, the acoustics cannot be optimized based on the behavior of the processor temperature. If FSC is based only on the digital thermal sensor, sustained temperatures above $T_{CONTROL}$ drive fans to maximum RPM. If FSC is based both on the ambient and digital thermal sensor, ambient temperature can be used to scale the fan RPM controlled by the digital thermal sensor. This would result in an optimal acoustic performance. Regardless of which scheme is employed, system designers must ensure that the thermal profile specification is met.

5.3.3 Thermal Excursion Power

Under fan failure or other anomalous thermal excursions, processor temperature (either T_{CASE} or DTS) may exceed the thermal profile for a duration totaling less than 360 hours per year without affecting long term reliability (life) of the processor. For more typical thermal excursions, the thermal monitor is expected to control the processor power level as long as conditions do not allow the processor to exceed the temperature at which Thermal Control Circuit (TCC) activation initially occurred.

Under more severe anomalous thermal excursions when the processor temperature cannot be controlled at or below thermal profile by TCC activation, then data integrity is not assured. At some higher thresholds, THERMTRIP_N will enable a shut down in an attempt to prevent permanent damage to the processor.

§

6 System Design Considerations

When designing a thermally capable system, all critical components must be simultaneously considered. The responsible engineer must determine how each component will affect another, while ensuring target performance for all components. The term “target performance” is used because some components (for example, LRDIMM) have better performance, depending on how well they are cooled. The system design team must set these target performance goals during the design phase so that they can be achieved with the selected component layout.

The location of components and their interaction must be considered during the layout phase. For example, memory that is heated by a processor will have worse performance than a layout that does not shadow memory behind a processor.

Although the memory components have fixed thermal specifications, the performance management of RDIMM will limit memory throughput to ensure that the temperature limits are met. Consequently, a poorly cooled memory subsystem will have worse performance. The processor is somewhat different in that it enables full performance at all times, as defined by its specifications. The thermal engineer’s responsibility is to ensure that each and every component meets its performance goals bounded by thermal and acoustic specifications but also computing performance such as memory throughput.

The thermal engineer directly influences the critical thermal parameters affecting processor cooling capability. For a given heatsink and retention solution, the layout and air-mover selection must ensure that all thermal specifications are met. It is desirable to drive chassis air temperature rise as low as reasonably possible while maximizing flow to each component. However, higher chassis temperature rise can be accommodated as long as the design implements a countering flow increase. These trade-offs are essential in designing a thermally capable system.

The number, size, and position of fans, vents, and other heat-generating components determine the component thermal performance and the resultant local ambient and airflow to the processor. The size and type (passive or active) of the thermal solution and the amount of system airflow can be traded off against each other to meet specific system design constraints.

In choosing the boundary conditions for a passive heatsink, the following methodology is recommended to ensure that a system can deliver the required boundary conditions. The Intel reference solution was developed by considering various system implementations to ensure that the boundary conditions were within reason.

- Conceptualize the layout with the system architect, including approximate volumetric constraints for the heatsink.
- Select air movers that will deliver airflow and local temperatures within reason to all system components (also account for T_{RISE} across the air-movers).
- Create a Computational Fluid Dynamics (CFD) model of the system.
- Run the CFD model with varying flow resistance representing the finned section of the heatsink.
- Extract an effective air-mover curve from the CFD results.
- Optimize the heatsink (fin thickness, quantity, base thickness, and so on) based on the effective air-mover curve.

- Determine whether that optimized thermal solution can meet processor specifications.
- Iterate through the previous steps to find a solution that will meet thermal requirements.

To develop a reliable and cost-effective thermal solution, thermal characterization and simulation should be carried out at the entire system level, accounting for the thermal requirements of each component. In addition, acoustic noise constraints may limit the size, number, placement, and types of air-movers that can be used in a particular design. A number of collaterals, such as thermal and mechanical models, are made available to aid in performing system and component level thermal characterizations. See Table 1-1 for the listing of available collaterals.

6.1 PCB Design Consideration

6.1.1 Allowable Board Thickness

The components described in this document (namely retention mechanism, backplate and the heatsink) will support board thickness in the range of 1.6 - 2.36 mm (0.063"-0.093") and 2.36 - 3.3 mm (0.093" - 0.130"). The studs on the backplate will need to be changed for longer ones if using the thicker board range (2.36 - 3.3 mm). Boards (PCBs) not within this range may require modifications to the backplate and the bolster plate.

Note: The dimensions presented in here do not account for a +/- 10% tolerance in them. For the max./min. values, refer to the corresponding backplate drawings.

6.1.2 Board Layout

Intel processors are targeted for use in a variety of board layouts and system form factors. Included in the list of system form factors are 1U, 2U, and workstation systems. Board layout varies within each system. Typical board layouts included shadowed configuration by which processors are placed in line or staggered with respect to direction of air flow. As an alternative processors may be placed side by side on the board.

6.1.3 Board Keep-Outs

Each of the components described in this document require an area beyond its physical size to accommodate components movement for installation purposes as well as to address their movement during shock and vibration. In identifying the board keep-outs, consider also board and system assembly process and tools. As a reference, recommended board keep-outs drawings (PCB top and bottom side) for the LGA3647 socket, retention mechanism, and heatsink are made available and included in the components assembly drawing. PCB keep-outs includes retention mechanism attach hole locations and sizes, components height limits in vicinity of the socket, as well as recommended area to allow access to retention and socket for processor installation

6.1.4 Silkscreen Marking Identifying Socket and Keep-Out Area

Intel is recommending the socket name be silk screened adjacent to the socket such that it is visible after the bolster plate is installed.

6.1.5 Board Deflection

Excessive board deflection may result in failure at socket solder joints. Keeping the board deflection under the socket to an acceptable level by adhering to the following conditions can reduce the risk of solder joint failure:

1. Using the Intel reference heatsink retention and backplate
2. Maintaining compliance to maximum load values

Placement of board-to-chassis mounting holes also impacts board deflection and resultant socket solder ball stress. Customers need to assess shock for their designs as their heatsink retention, heatsink mass and chassis mounting holes may vary.

Designs that do not meet the design objectives of the backplate or exceed the maximum heatsink static compressive load, should follow Board Deflection Measurement Methodology as outlined to assess risk to socket solder joint reliability.

6.1.6 Socket Land Pattern Guidance

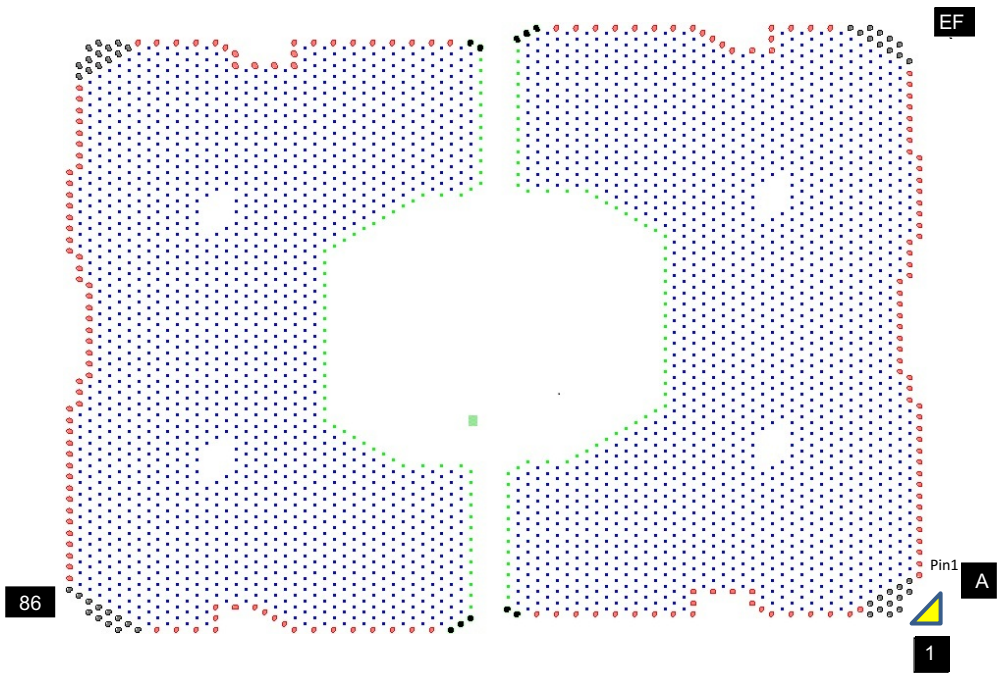
The land pattern guidance provided in this section applies to printed circuit board design. The Recommendation for Printed Circuit Board (PCB) land patterns is to ensure solder joint reliability during dynamic stresses, often encountered during shipping and handling and hence to increase socket reliability.

The land pattern for the LGA3647-0 socket is a 39 mil hexagonal array. See Figure 6-1 for detailed location and land pattern type.

Table 6-1. LGA3647 Socket Land Pattern Guidance

Parameter	Value
Component Size	76.12 mm x 60.5 mm
Pitch	0.859 mm in X, and 0.991 mm staggered in Y
Pkg SRO	0.56 mm in X, and 0.854 mm in Y
Stencil Opening	19 mil
Ball Count	3647
LPID	2725

Figure 6-1. LGA3647 Socket Land Pattern Guidance



Leg end	Color	Pad Size (mils/microns), Type, & Trace Requirements	# of lands
●	Black	17x20 mil (431.8umx508um) **Oblong Pads (see definition below)** with 17mil (431.8um) pad opening offset by 1.5 mil – offset direction is towards the inside of the socket. **These should be partial (roughly half) SMDs (full SMD or full MD is NOT acceptable)** Preferred: Long axis of pad and traces connected to the pad should be pointing away from the center of the pin field (45°/135° wrt socket edge). Alternate: Long axis of pad and traces connected to the pad pointing along the skt vertical or horizontal axis	58
●	Red	17x20 mil (431.8umx508um) **Oblong Pads** with 17mil (431.8um) pad opening. **These should be partial (roughly half) SMDs (full SMD or full MD is NOT acceptable)**. Long axis of pad and traces connected to the pad should be pointing away from the center of the pin field(90° wrt socket edge) – Vertical on North-South edges and Horizontal on East-West edges	176
●	Green	Between 17mil (431.8um) to 20mil (508um) circular **MD (see definition below). Larger pads are preferred**	130
●	Blue	Preferred: 17mil (431.8um) circular **MD (see definition below) OR** Alternate: **SMD** with 17mil (431.8um) pad opening	3283
		Total =	**3647**

Pad Type Recommendation

Intel defines two types of pad types based on how they are constructed. A Metal Defined (MD) pad is one where a pad is individually etched into the PCB with a minimum width trace exiting it. The solder mask defined (SMD) pad is typically a pad in a flood plane where the solder mask opening defines the pad size for soldering to the component.

In thermal cycling a MD pad has shown to be more robust than a SMD pad type. The solder mask that defines the SMD pad can create a sharp edge on the solder joint as the solder ball/paste conforms to the window created by the solder mask.

For certain failure modes, the MD pad may not be as robust in shock and vibration (S and V). During S and V, the predominant failure mode for a MD pad in the corner of the BGA layout is pad craters and solder joint cracks. A corner MD pad can be made more robust and behave like a SMD pad by having a wide trace enter the pad. This trace should be 10 mil minimum but not to exceed the pad diameter and exit the pad.

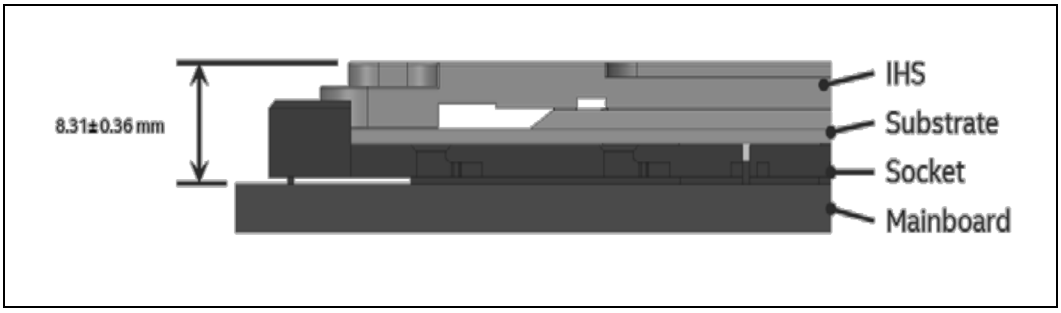
During board flexure that results from shock and vibration a SMD pad is less susceptible to a crack initiating due to the larger surface area. Intel has defined selected solder joints of the socket as Non-Critical To Function (NCTF) when evaluating package solder joints post environmental testing.

The signals at NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.

6.2 System Mechanical Design Consideration

6.2.1 Processor and Socket Stack-up Height

Figure 6-2. Processor/Socket Stack Height



Overall processor and socket stack height is provided here as convenience and should be derived from (a) the height of the socket seating plane above the motherboard after reflow, (b) the height of the package from the package seating plane to the top of the IHS, and accounting for its nominal variation and tolerances.

6.2.2 Components Volumetric

The baseboard keep-out zones on the primary and secondary sides and height restrictions under the enabling component region will be provided and included as a part of the components drawings. The overall volumetric keep in zone encapsulates the processor, socket, and the entire thermal/mechanical enabling assembly.

6.2.3 Components Mass

The static compressive load should also be considered in dynamic assessments.

Direct contact between backplate and chassis pan will usually help minimize board deflection during shock.

Table 6-2. Components Mass

Component	Mass	Notes
Processor	112 g	
Socket including PnP cover	29 g	Socket PnP cover mass is 6.5 g; Each socket half including PnP cover mass is 14.5 g
Top Plate Assembly	58 g	
Backplate	139 g	
Heatsink	600 g	Maximum allowable heatsink mass. Actual heatsink mass may vary based on heatsink size and design of the heatsink.

6.3 System Thermal Design Considerations

6.3.1 Ambient Temperature (TLA)

The temperature of the inlet air entering the processor is referenced in this document as the ambient temperature (T_{LA}). This is not a system requirement. It is measured from the air upstream and in close vicinity to the processor cooling device. For the cooling systems, the ambient temperature is measured from the inlet air to the cooling device.

6.3.2 Airflow

Airflow should be provided by a system fan or blower to cool the processor package. Available airflow at the component's cooling solution, direction, and restrictions through the system should be considered in optimizing the components cooling solution design.

6.3.3 Pressure Drop (Delta P)

The allowable pressure drop in the airflow to ensure cooling requirements for the system components at downstream from the processor should be taken into account in designing the processor cooling requirements.

§

7 Thermal Design Guidelines

7.1 Heatsink Design Considerations

To remove the heat from the processor, basic thermal design considerations include:

- The area of the surface on which the heat transfer takes place - Without any enhancements, this is the surface of the processor package IHS. One method used to improve thermal performance is to attach a heatsink to the IHS. A heatsink can increase the effective heat transfer surface area by conducting heat out of the IHS and into the surrounding air through fins attached to the heatsink base.
- The conduction path from the heat source to the heatsink fins - Providing a direct conduction path from the heat source to the heatsink fins and selecting materials with higher thermal conductivity typically improves heatsink performance. The length, thickness, and conductivity of the conduction path from the heat source to the fins directly impacts the thermal performance of the heatsink. In particular, the quality of the contact between the package IHS and the heatsink base has a higher impact on the overall thermal solution performance. Thermal Interface Material (TIM) is used to fill in the gap between the IHS and the bottom surface of the heatsink, and thereby improves the overall performance of the thermal stack-up (IHS-TIM-Heatsink). With extremely poor heatsink interface flatness or roughness, TIM may not adequately fill the gap. The TIM thermal performance depends on its thermal conductivity as well as the pressure load applied to it.
- The heat transfer conditions on the surface upon which heat transfer takes place - Convective heat transfer occurs between the airflow and the surface exposed to the flow. It is characterized by the local ambient temperature of the air, T_{LA}, and the local air velocity over the surface. The higher the air velocity over the surface, the more efficient the resulting cooling. The nature of the airflow can also enhance heat transfer via convection. Turbulent flow can provide improvement over laminar flow. In the case of a heatsink, the surface exposed to the flow includes the fin faces and the heatsink base.

An active heatsink typically incorporates a fan that helps manage the airflow through the heatsink.

Passive heatsink solutions require in-depth knowledge of the airflow in the chassis. As the heatsink fin density (the number of fins in a given cross-section) increases, the resistance to the airflow increases; it is more likely that the air will travel around the heatsink instead of through it, unless air bypass is carefully managed. Using air-ducting techniques to manage bypass area is an effective method for maximizing airflow through the heatsink fins.

7.2 Thermal Interface Material (TIM) Considerations

Thermal interface material between the processor IHS and the heatsink base is necessary to improve thermal conduction from the IHS to the heatsink. Many thermal interface materials can be pre-applied to the heatsink base prior to shipment from the heatsink supplier without the need for a separate TIM dispense or attachment process in the final assembly factory.

All thermal interface materials should be sized and positioned on the heatsink base in a way that ensures that the entire area is covered. It is important to compensate for heatsink-to-processor positional alignment when selecting the proper TIM size.

When pre-applied material is used, it is recommended that it have a protective cover.

Thermal performance usually degrades over the life of the assembly and this degradation needs to be accounted for in the thermal performance. Degradation can be caused by shipping and handling, environmental temperature, humidity conditions, load relaxation over time, temperature cycling or material changes (most notably in the TIM) over time. For this reason, the measured T_{CASE} value of a given processor may increase over time, depending on the type of TIM material.

7.3 Thermal Solution Performance Characterization

The case-to-local ambient Thermal Characterization Parameter (Ψ_{CA}) is defined by:
$\Psi_{CA} = (T_{CASE} - T_{LA}) / TDP$

Where:

T_{CASE} = Processor case temperature (°C)

T_{LA} = Local ambient temperature before the air enters the processor heatsink (°C)

TDP = TDP (W) assumes all power dissipates through the integrated heat spreader. This inexact assumption is convenient for heatsink design.

$\Psi_{CA} = \Psi_{CS} + \Psi_{SA}$

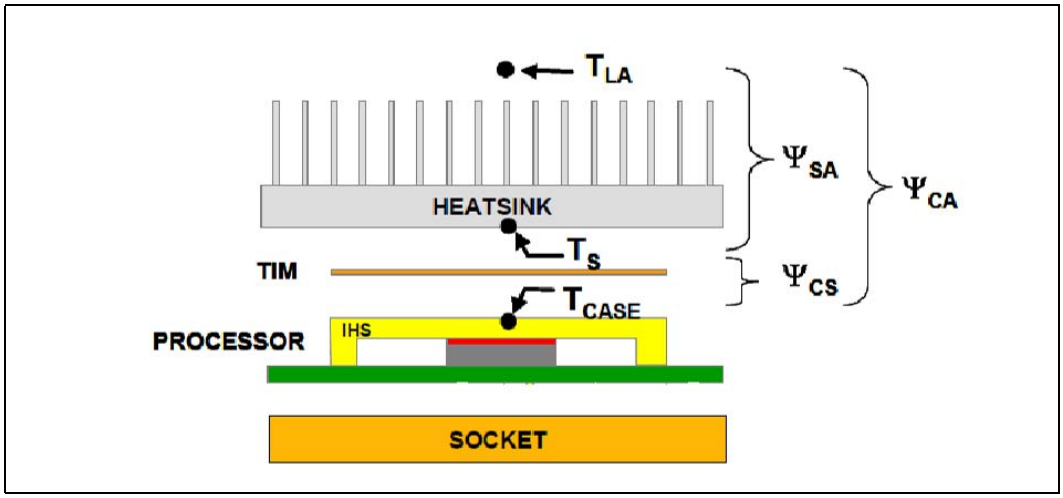
Where:

Ψ_{CS} = Thermal characterization parameter of the TIM (°C/W) is dependent on the thermal conductivity and thickness of the TIM.

Ψ_{SA} = Thermal characterization parameter from heatsink-to-local ambient (°C/W) is dependent on the thermal conductivity and geometry of the heatsink and dependent on the air velocity through the heatsink fins.

Figure 7-1 illustrates the thermal characterization parameters.

Figure 7-1. Thermal Characterization Parameters



§

8 Processor Heatsink Module and Loading Mechanism Design Guide

Processor enabling components consist of a set of mechanical components that enable integration of the processor with the board and system. Unlike the previous generation of LGA sockets, the LGA3647-0 socket uses a spring-loading mechanism to maintain the interface between the processor and the socket. The socket loading spring is provided by the bolster plate and its design is defined to provide the socket static load. The heatsink retention mechanism provides the board with structural stiffness to secure and support the mass the heatsink. In preventing damage to the socket during the processor installation, the processor and heatsink are held together using a package carrier mechanism. The assembly of the processor and heatsink prior to socket installation is referred to as the Processor Heatsink Module (PHM).

The main components of the socket stack are:

- Backplate
- Bolster plate with spring
- Processor package carrier or carrier
- Heatsink

8.1 PHM Overview

The LGA3647-0 socket PHM design consists of a assembly of the processor, heatsink, and a package carrier. The PHM design enables ease of installation of the processor into the socket while utilizing the guide posts of the bolster plate to pre-align the PHM and socket in minimizing risk of the damaging the socket contacts.

Figure 8-1. LGA 3647-0 Enabling Components (ISO View)

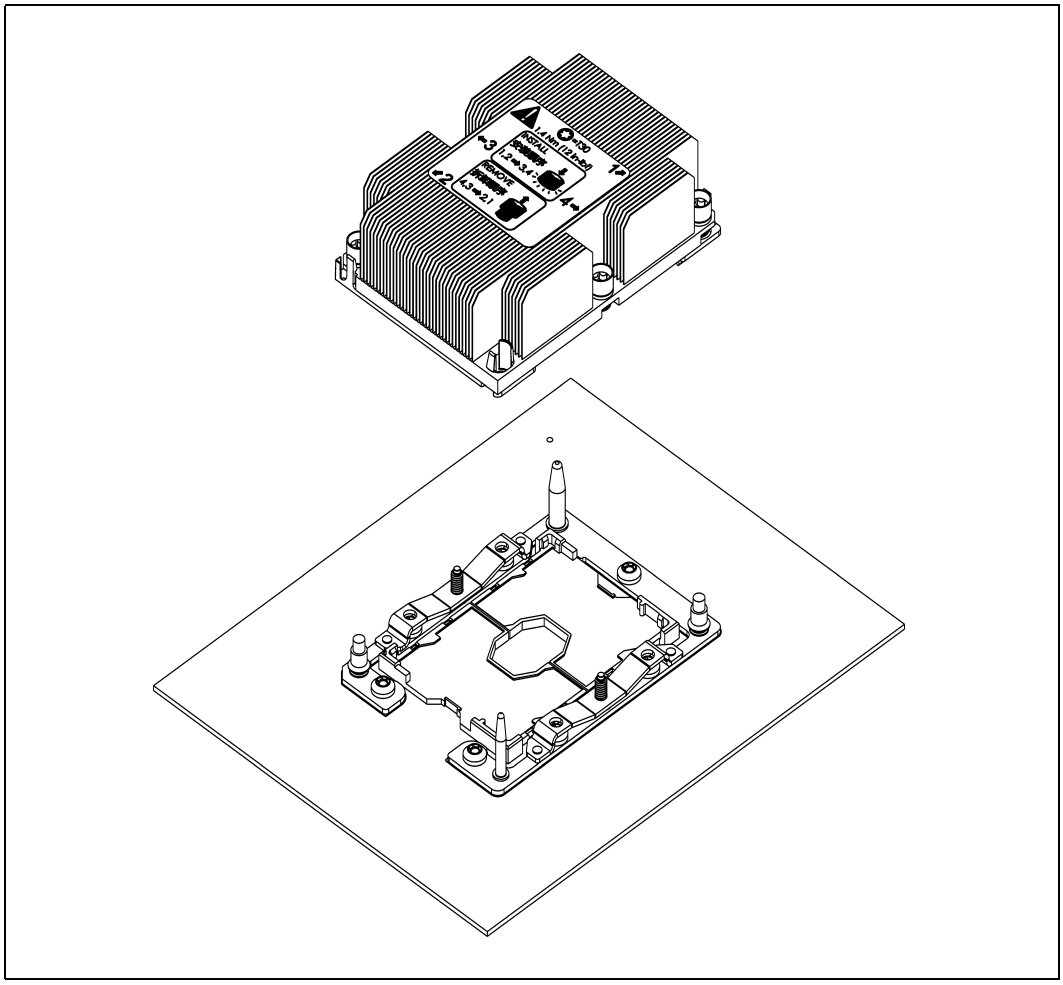
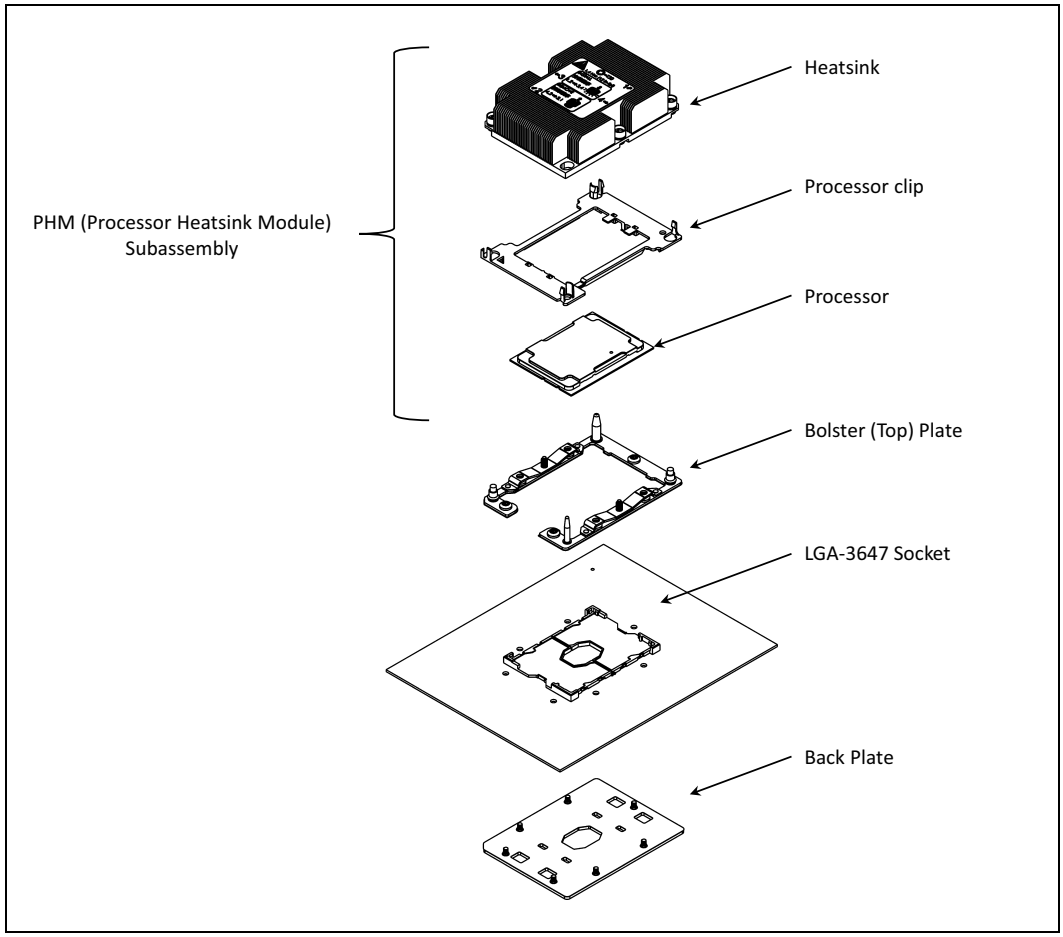


Figure 8-2. LGA3647-0 Enabling Components (Exploded View)



8.2 PHM Mechanical Design Considerations and Recommendations

8.3 PHM Features

One of the key features of the PHM is enabling the integration of the processor and heatsink as a single module. As a module, the PHM assembly acts as the vehicle for installing the processor onto the socket; reducing the risk of damaging the socket contacts.

Bolster plate guide posts serve as the alignment feature between the PHM and socket. Dissimilar posts on the bolster plate are the keying feature between the socket and the PHM that prevents the PHM from engaging with the socket when incorrectly oriented.

Protrusions on four corners of the package on the package carrier provide secondary alignment between the PHM and the socket as they interface with the socket wall exterior. Primary alignment between processor and socket is achieved through socket wall interior by constraining the processor movement.

8.4 PHM Loading Mechanism (PHLM)

8.4.1 Retention Mechanism Design Overview

The LGA3647 socket retention mechanism design consists of a top (bolster) plate and a backplate.

Bolster Plate with Spring

The bolster plate is an integrated subassembly that includes two corner guiding posts placed at opposite corners, nuts to mate with the backplate, and two springs that attach to the heatsink via screws. The corner posts guide the Processor Heatsink Module (PHM) as it is lowered over the socket. The corner posts act as coarse position constraints in the X-Y direction to prevent the PHM from moving and potentially damaging the processor package or socket. The springs on either side of the bolster plate are mechanically attached via rivets. The PHM is secured to the bolster plate by the two screws located in mid section on either side of the heatsink. Doing so will exert force normal to the socket at the top of the package IHS. The resulting socket-to-processor contact force ensures maximum contact areas between socket pins and processor package lands, as well as thermal interface material bond between package and heatsink. The springs include stoppers on their outer edges, to prevent movement of the heatsink in the Z-direction due to forces parallel to the motherboard.

Backplate

The backplate provides structural rigidity to the motherboard supporting the PHM mass and reducing board deflection resulted form socket loading. Bolster plate cut-outs enables component placements on the backside of the motherboard. The backplate is secured to the bolster plate at its threaded PEM studs.

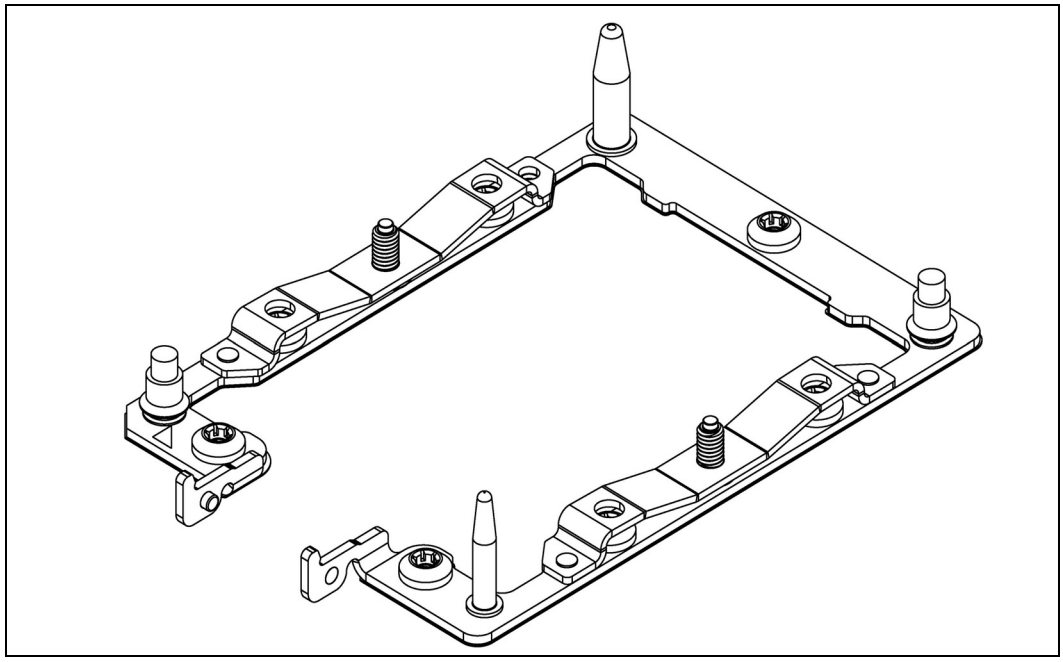
Note: The backplate is compatible only with the matching bolster plate.

Both bolster plate and the backplate are isolated from the routing and vias on the backside of the motherboard by an insulator covering entire surface interface between the plates and the motherboard.

Nut Durability Specification

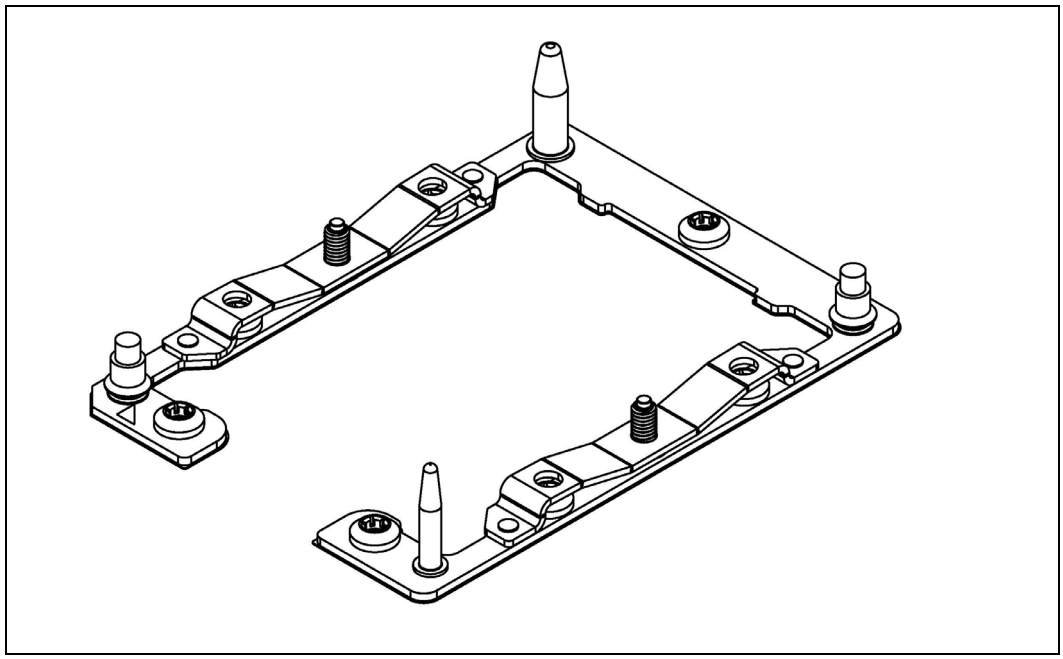
The PHLM heatsink nuts and bolster plate studs are rated to a durability specification of 12 installation and removal cycles, when using the reference designs with lubrication. Lubrication is required on the bolster plate threaded studs and heatsink nut threads. This is based on the visual inspection criteria of no observed dust/shavings greater than 0.5 mm in length as seen from the naked eye from 24 inches away with direct overhead lighting under cool white fluorescent light conditions [60-120 Ft-Candle (645-1293 LUX)] or equivalent, and a viewing time of one visual pass of 5-7 seconds for each surface. Refer to Appendix D, “Retention Assembly Mechanical Drawings” for details on the hardware.

Figure 8-3. Narrow Fabric Bolster Plate Assembly (ISO View)



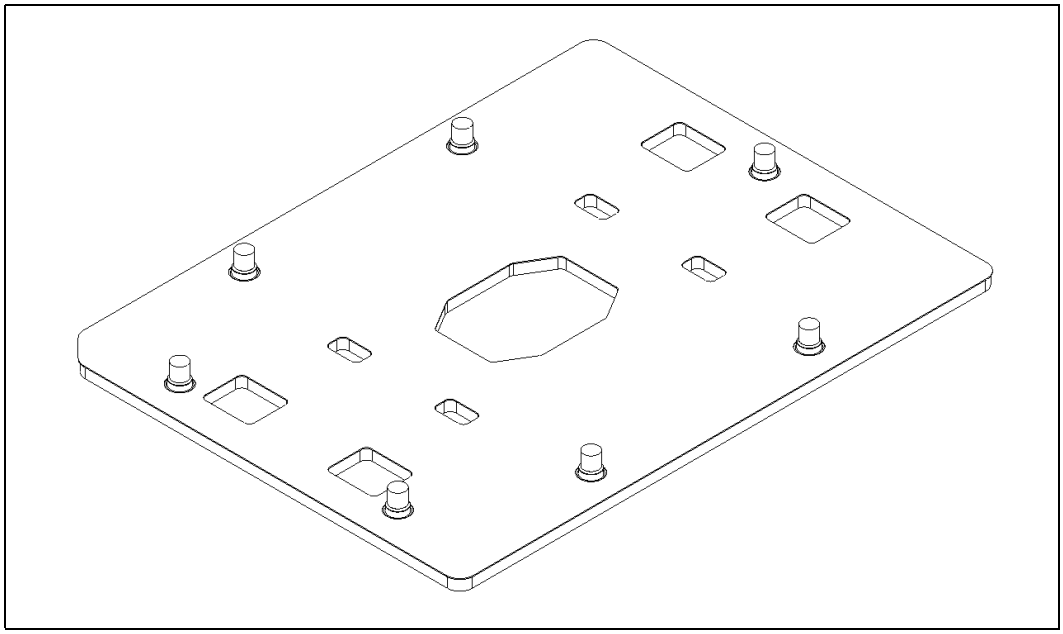
Note: Narrow fabric bolster plate design includes features required for retention of Intel fabric passive cable. Even though the Second Generation Intel® Xeon® Scalable Processors does not support the use of the Intel fabric passive cable, it is possible to use the narrow fabric bolster plate for the PHLM.

Figure 8-4. Narrow Non-Fabric Bolster Plate Assembly (ISO View)



Note: Narrow non-fabric bolster plate design does not include the features required for retention of the Intel fabric passive cable.

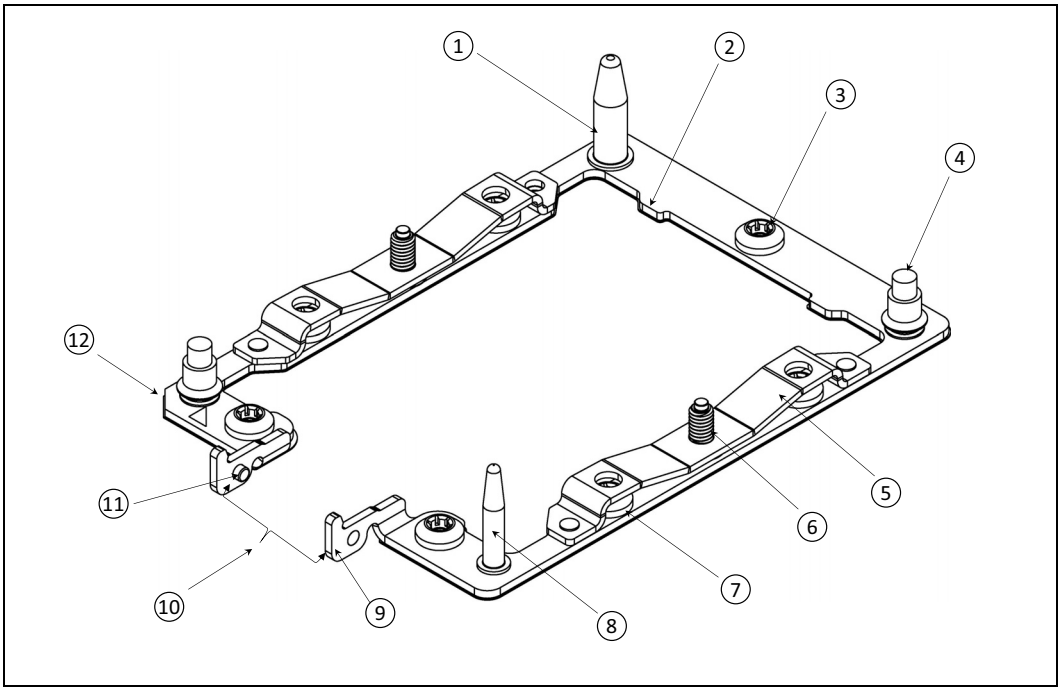
Figure 8-5. Narrow Backplate Assembly (ISO View)



8.4.2 PHLM Features

The bolster plate incorporates mechanical features specific to Second Generation Intel® Xeon® Scalable Processors PHM and PCB. The large and small guide posts provide both a keying mechanism and serve as a secondary alignment between the PHM and socket.

Figure 8-6. Narrow Bolster Plate Part Feature



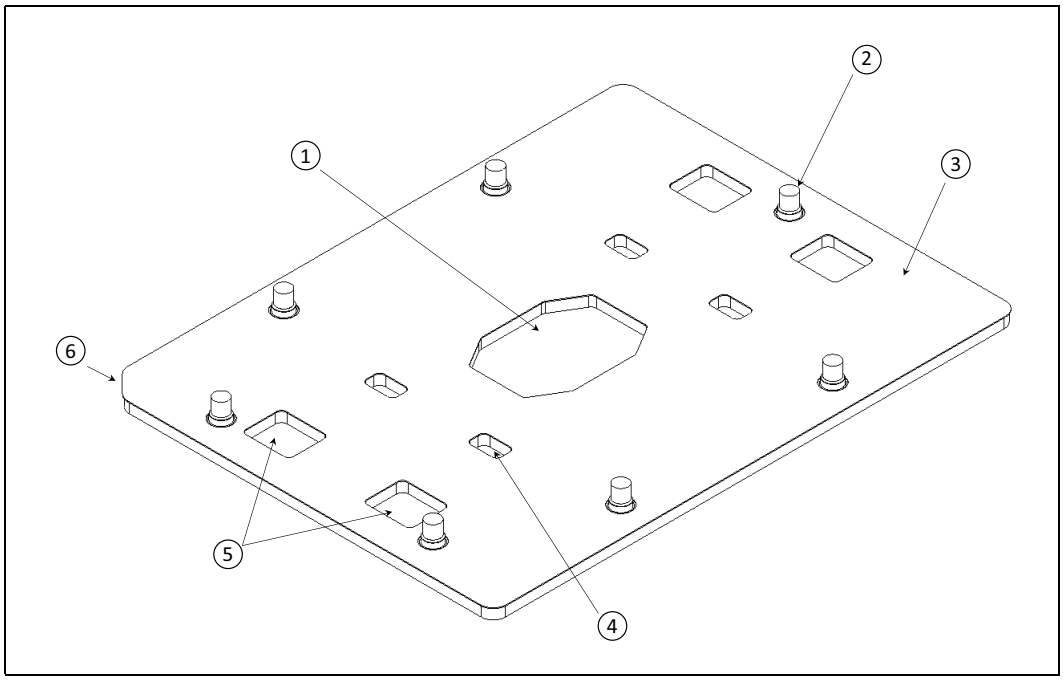
Narrow Bolster Plate

1. PHM guide post (large)
2. Positioning tab (with respect to socket)
3. Attachment fasteners (7x)
4. PEM threaded studs (2x)
5. Load spring (heatsink attach spring)
6. Load screw (heatsink attach screw -2x)
7. Insulator
8. PHM guide post (small)
9. LEC54B connector latch (not supported in the Second Generation Intel® Xeon® Scalable Processors)
10. LEC54B connector opening (not supported in the Second Generation Intel® Xeon® Scalable Processors)
11. LEC54B guide pin (not supported in the Second Generation Intel® Xeon® Scalable Processors)
12. Pin one indicator

Note: The narrow Fabric bolster plate can be used with the Second Generation Intel® Xeon® Scalable Processors , although items 9, 10 and 11 will not have any added value as the

LEC54B connector is not enabled in this generation. For a bolster plate without these features, refer to the Non-Fabric Narrow Bolster Plate.

Figure 8-7. Narrow Backplate Part Feature



Narrow Backplate

1. Center cavity for PCB components
2. PEM studs (7x)
3. Insulator
4. Cavity for PCB components (small - 4x)
5. Cavity for PCB components (square - 4x)
6. Pin one indicator

8.4.3 PHM Loading Mechanism Material Specifications

PHM retention mechanism is defined to be installed onto the PCB post socket assembly process. There are no system attachment. However, additional support may be necessary depending on board and system configuration and the heatsink mass.

Table 8-1. Bolster Plate Material Specifications

Parameter	Value	Notes
Material Thickness	1.5 ± 0.08 mm	
Insulator Thickness	0.18 +0.05/-0.02 mm	
Material Strength	Tensile Yield: 758 MPa	
	Modulus of Elasticity Ultimate: 193 GPa	
Flatness	1.0 mm	
Spring Rivet Pullout Force	500 N min	
Nut/Collar Separation Force	222 N min	

Note: See bolster plate drawing for additional details.

Table 8-2. Backplate Material Specifications

Parameter	Value	Notes
Material Thickness	2.2 ±0.05	
Insulator Thickness	0.178 +0.051/-0	
Material Strength	Tensile Yield: 250 MPa min Ultimate Tensile Strength: 300 MPa min	
Flatness	0.2 mm	
Studs pull-out Force	667 N	
Studs Torque Out	2.25 N-m min	

Note: See backplate drawing for details.

8.4.4 Bolster and Backplates Marking

All markings required in this section must withstand a minimum temperature of 100 °C.

Table 8-3. Bolster and Backplates Traceability

Part Number	• Manufacturer's Insignia (font size at supplier's discretion). • Both part number and manufacturer's insignia will be visible when assembled with the processor and the heatsink.
Lot Traceability	• Each component will be marked with a lot identification code to allow traceability of all components, date of manufacture (year and week), and assembly location. The marking on the plates must be placed on a surface that is visible after installed onto the PCB. In addition, this identification code must be marked on the exterior of the box in which the unit is shipped.

8.5 Package Carrier Design

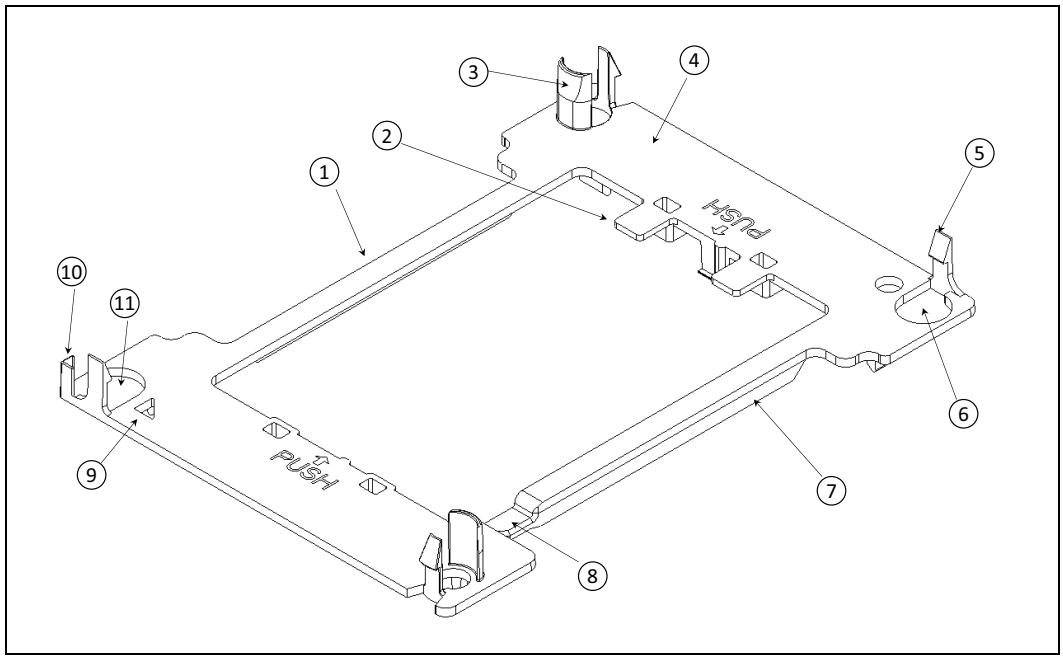
The processor package carrier or carrier is an integral part of the Processor Heatsink Module (PHM). It holds the package and heatsink together creating a single module for installation onto the socket. Matching the package carrier designated keying features to the processor package notches ensures the package is properly aligned to the package carrier. The PHM package carrier is designed to align the processor to the socket using socket walls as alignment features. Alignment between the package carrier and socket provides a secondary level of alignment in preventing damage to the socket during the processor installation sequence.

During the components subassembly, the processor package is first aligned and latched onto the package carrier. The pre-assembled processor and package carrier is then attached and held to the processor heatsink. Thermal Interface Material (TIM2) is expected to be pre-applied to the heatsink prior to the package carrier plus processor subassembly installation.

8.5.1 Package Carrier Mechanical Features

Key features of the PHM package carrier are identified in the following illustrations.

Figure 8-8. Narrow Non-Fabric Package Carrier Mechanical Features (Top View)

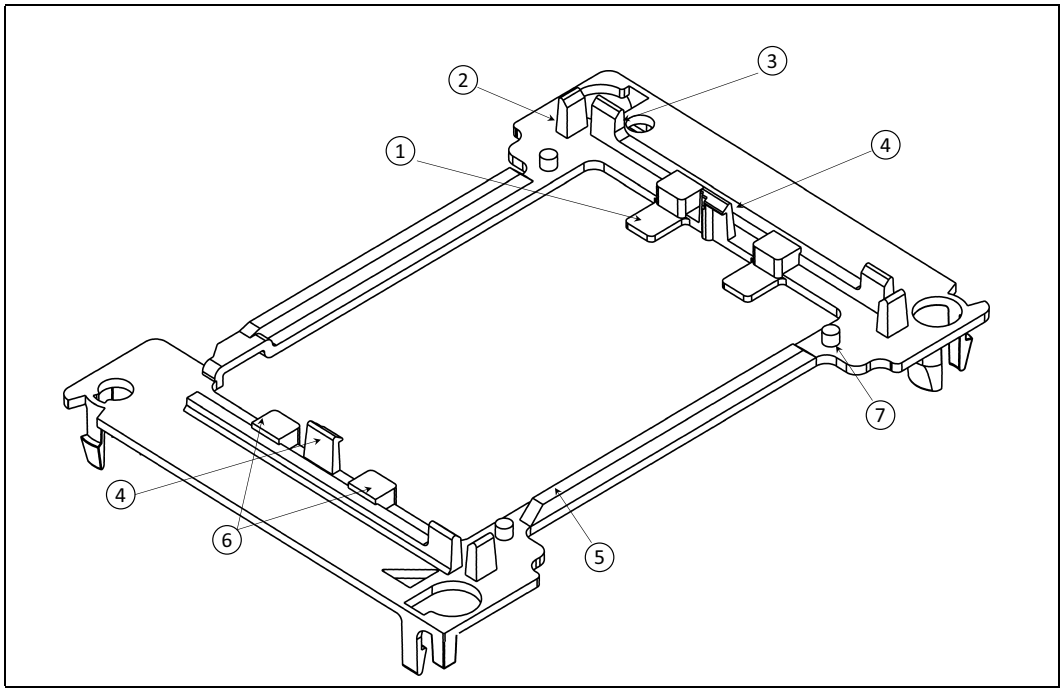


Note: The narrow non-fabric package carrier is not compatible with the processor SKUs with fabric feature.

Narrow Non-Fabric Package Carrier Mechanical Features (Top View)

1. Crossbar
2. Side walls limiting package movement
3. Heatsink alignment partial-post
4. Surface interface with the heatsink base
5. Heatsink latch (4x)
6. Package carrier to bolster plate small post alignment hole
7. Stiffening crossbar
8. Opening for the tool access (to break the TIM bonding between the processor and heatsink)
9. Pin one indicator
10. Carrier to heatsink orientation indicator
11. Package carrier to bolster plate large post alignment hole

Figure 8-9. Narrow Non-Fabric Package Carrier Mechanical Features (Bottom View)



Narrow Non-Fabric Package Carrier (Bottom View)

1. Package IHS interface
2. Package carrier to socket body alignment features
3. Package carrier to socket body alignment features
4. Package carrier latch
5. Stiffening crossbar
6. Package carrier latch at the processor tab
7. Prevention pillars to avoid the TIM breaker to enter a forbidden area (3x)

8.5.2 Package carrier Marking

All markings required in this section must withstand a minimum temperature of 100°C

Table 8-4. Package carrier Marking

Part Number	• Manufacturer's insignia (font size at supplier's discretion). • This mark will be molded or laser-marked into the top side of the socket housing. • Both part number and manufacturer's insignia will be visible when assembled with the processor and the heatsink.
Lot Traceability	• Package carrier shall be marked with a lot identification code to allow traceability of all components, date of manufacture (year and week), and assembly location. The mark must be placed on a surface that is visible after assembled with the processor and heatsink. In addition, this identification code must be marked on the exterior of the box in which the unit is shipped.

8.5.3 Package Carrier Material Specifications

Table 8-5. Package Carrier Material Specifications

Parameter	Value	Note
Type	PC-ABS	Recommended
Flammability	UL Flammability rating 94-V0	Required
Withstand Temperature	120 °C min.	Required

8.5.4 Package Carrier Durability

The package carrier must withstand 10 numbers of attachment/removal cycles. An attachment cycle is defined as a one time attachment of the carrier to the processor package and heatsink. Removal cycle is defined as separating the carrier from the processor and heatsink one time.

The package carrier must also withstand 10 numbers of socket installation/removal cycles. The Installation and removal cycle is defined as installing the PHM onto the socket, securing it, un-securing the PHM, and disengaging the PHM from the socket.

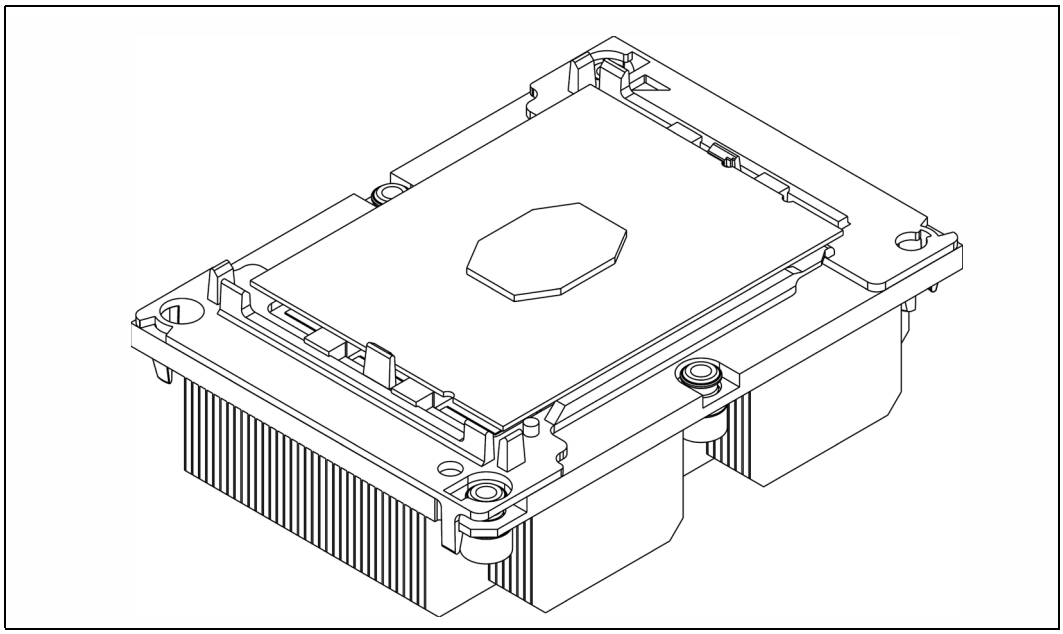
8.6 PHM Heatsink

The processor requires a heatsink to remove the heat dissipated at the processor package IHS and to maintain the processor die temperature within its operating temperature. The PHM heatsink design serves a dual purpose. One is to remove the heat from the processor. The other is to apply the required loading to actuate the LGA3647 socket and to apply a sufficient amount of pressure to maintain the bond between the TIM2, the heatsink pedestal, and the processor IHS.

Processor heatsink performance is dependent on the thermal environment it is in, such as inlet air temperature and flow rate and applied heatsink design technology. The heatsink thermal characteristics within a defined set of thermal boundary conditions must meet the processor thermal specifications for the processor to achieve its optimum performance.

The processor heatsink is designed to interface with the PHM package carrier and the socket retention mechanism. Mechanical features at the base of the heatsink enable the PHM to latch on and hold together the processor and the heatsink. Retention mechanism standoffs provide alignment and orientation with respect to the socket.

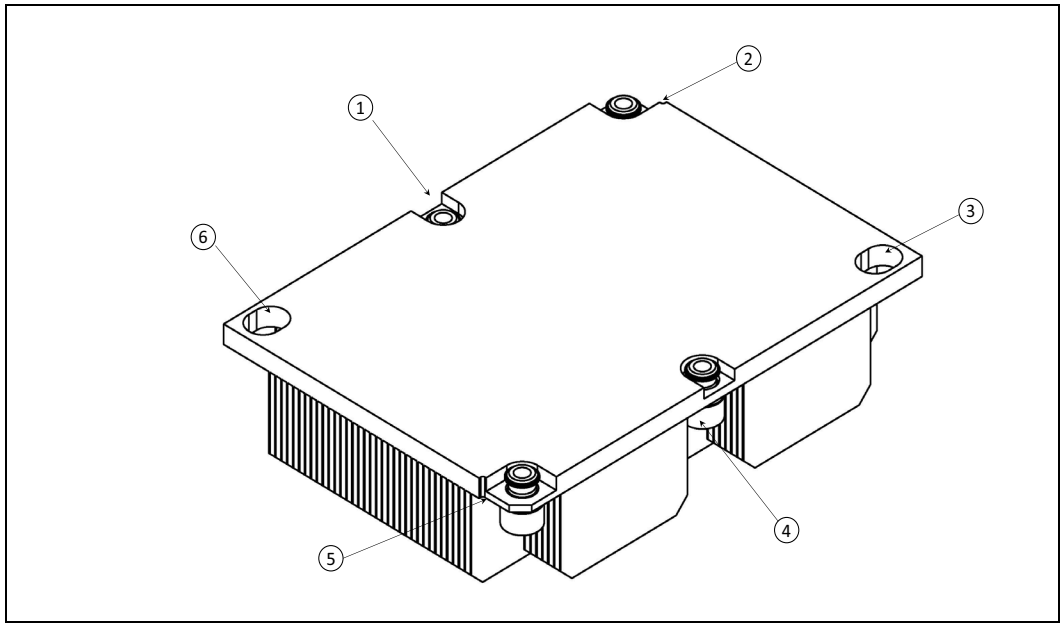
Figure 8-10. PHM Assembly (Bottom View)



Two fasteners on the sides of the heatsink secures the heatsink to the retention mechanism. When fasteners are tightened to the specified torque limit, the heatsink induces force normal to the socket through the processor package IHS. Not adhering to the package and the socket load specification can result in damaging the processor and/or the socket as well as the retention mechanism.

8.6.1 Heatsink Mechanical Interfaces

Figure 8-11. Heatsink Base Mechanical Features



Heatsink Mechanical Features

1. Bolster plate spring load fastener (left side)
2. Heatsink retention fastener
3. Heatsink to bolster plate post alignment hole
4. Bolster plate spring load fastener (right side)
5. Cut-out for package carrier to heatsink latching feature
6. Heatsink to bolster plate post alignment hole

8.6.2 Heatsink Mechanical Requirements

Mechanical features of the heatsink are defined such that they enable integration of the processor and the package carrier to establish a processor heatsink module. Hence, it is critical that the initial position of the processor with respect to the heatsink base is well controlled. This is established through the package carrier and through the carrier to heatsink latching positions.

The heatsink is also used to establish the preliminary alignment between the processor and the socket. Processor to socket preliminary alignment is established through bolster plate alignment posts which also act as a keying feature ensuring the PHM is properly orientated with respect to the socket.

The four fasteners on the heatsink are used to secure the PHM to the bolster plate. Two of the fasteners in the corners of the heatsink, diagonal to each other, are used to secure the heatsink to the bolster plate. These fasteners must be tightened first to ensure the heatsink has touched-down on the bolster plate, and it is leveled to the bolster plate. This will 1) reduce the risk of damaging contacts during the installation, and 2) ensures heatsink and bolster plate load fasteners are close to engage. Properly

torquing the two middle fasteners will provide the loading necessary to actuate the socket while complying with both the socket and processor mechanical loading specifications.

Heatsink base cutouts for the package carrier latching features and for the fasteners are defined to address the heatsink mechanical and integration requirements. Refer to the heatsink mechanical drawing for details.

Table 8-6. Heatsink Mechanical Requirement

Parameter	Values	Notes
Heatsink Base Thickness	4.5 ±0.12 mm	See heatsink mechanical drawings.
Heatsink Base Flatness	0.24 mm	
	0.077 mm	TIM interface area centered on heatsink base
Bolster plate small hole dimensions for the bolster plate alignment post	See heatsink mechanical drawings.	
Bolster plate large hole dimensions for the bolster plate alignment post	See heatsink mechanical drawings.	
Heatsink base holes dimensions for the bolster plate spring fasteners	See heatsink mechanical drawings.	
Heatsink base holes dimensions for the bolster plate retention fasteners	See heatsink mechanical drawings.	
Bolster Plate retention Fastener Torque	8.0 in-Lb	
Heatsink Installation Torque	12.0 in-Lb	
Maximum Allowable Heatsink Mass	600 g.	

Note: This stiffness guidance is related to socket reliability, not thermal performance. Any potential thermal impact due to heatsink base deflection at lower stiffness levels needs to be determined separately.

§

9 Component Assembly Instructions

Reference enabling components are designed for compatibility with the Second Generation Intel® Xeon® Scalable Processors package and to ease board and system assembly. The processor enabling solution is illustrated in Figure 9-1, "Processor and Enabling Components Mechanical Assembly" on page 85. The method of installing the processor onto the motherboard is to assemble the processor and its enabling solution prior to installation onto a board. This will allow the processor and its cooling solution to be assembled offline and delivered to the board or the system assembly site. This method is commonly referred to as the pre-attach method. In this section pre-assembling the processor and the heatsink as a module (PHM) and its installation onto the motherboard will be described. It should be noted that without the processor package carrier, there is no control mechanism to secure the processor to the heatsink or align the module to the socket.

The processor and its enabling components assembly are divided into three areas. First is the top and bottom plate installation onto the motherboard. Second is the processor, and its cooling solution assembly. Last is the processor installation onto the socket and securing the assembly to the board.

Instructions provided from here on are an overview of the components assembly and installation onto a board or a system.

9.1 Processor Enabling Components

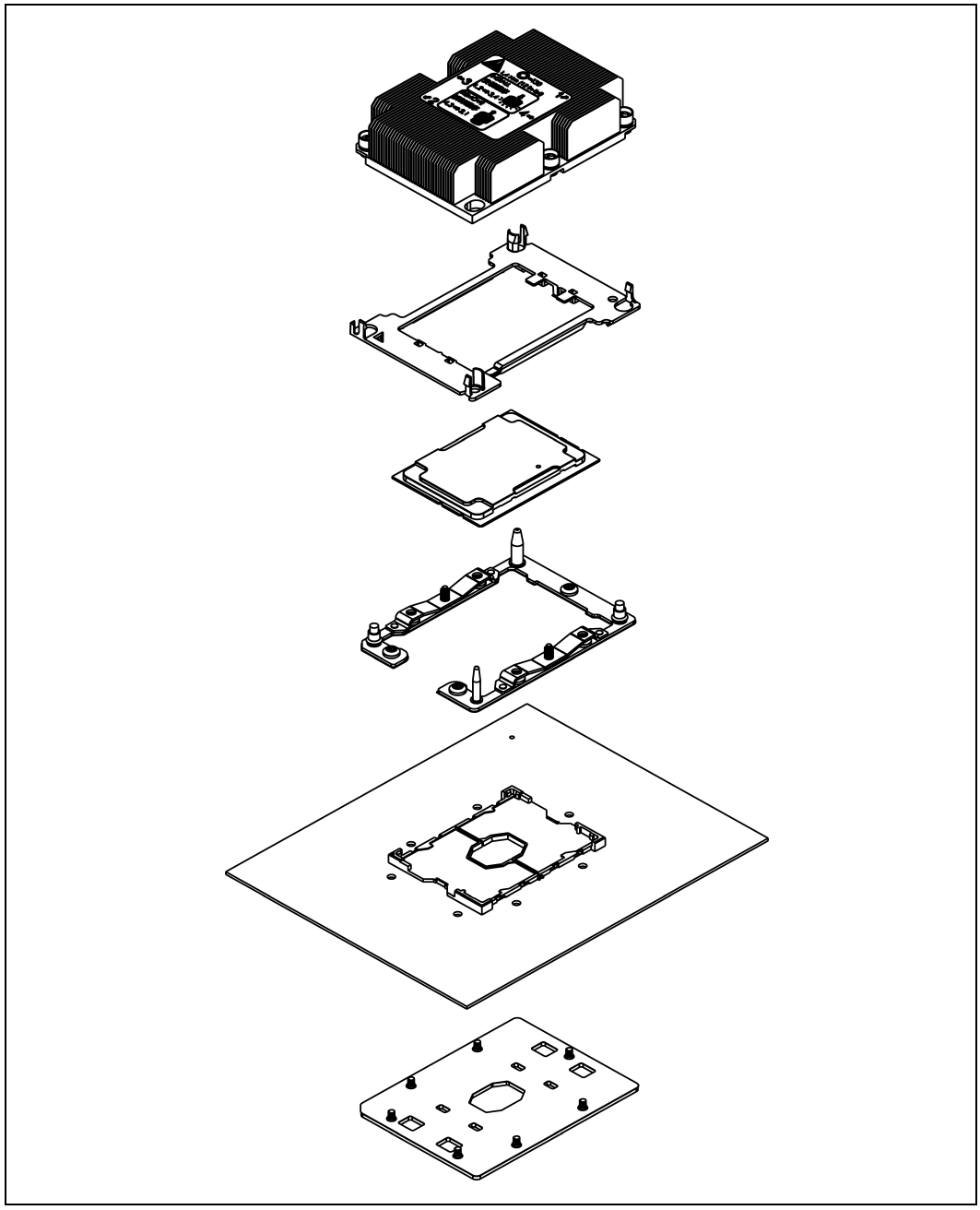
Processor enabling components consist of a set of components that enable integration of the processor with the board and system. Processor enabling components are listed in Table 9-1, "LGA3647-0 Components Listing and Compatibility" and are illustrated in Figure 9-1, "Processor and Enabling Components Mechanical Assembly".

Table 9-1. LGA3647-0 Components Listing and Compatibility

Enabling Component	Narrow Non-Fabric PHM
Processor Package	Non-fabric
LGA3647-0 LGA socket (Socket P0)	Yes
Narrow Fabric PHLM	
Narrow Backplate*	Yes
Narrow Fabric Bolster Plate	Yes
Narrow Fabric Socket Dust Cover	Yes
Narrow Fabric Bolster and Socket Dust Cover	Yes
Narrow Fabric Package Carrier	No
Narrow Non-Fabric PHLM	
Narrow Backplate*	Yes
Narrow non-fabric Bolster Plate	Yes
Narrow non-Fabric Socket Dust Cover	Yes
Narrow non-Fabric Bolster Socket Dust Cover	Yes
Narrow non-Fabric Package Carrier	Yes
Square PHLM	
Square Bolster Plate*	No
Square Socket Dust Cover	No
Square Bolster Socket Dust Cover	No
Square Backplate	No
Square Package Carrier	No
Heatsinks	
1U Heatsink High Performance	Yes
1U Low Impedance Heatsink	Yes
2U Narrow Heatsink	Yes
Tower Square Heatsink	No
Non-MCP (10-Year Use + NEBS-Friendly) Profile	Yes

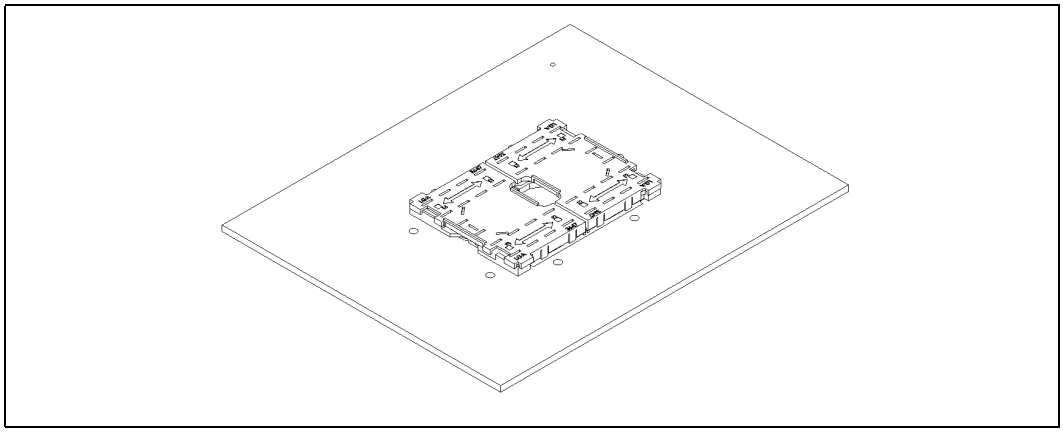
Notes:
1. The components marked with an * support board thickness of 1.6 - 2.36 mm (0.063” - 0.093”).
2. Refer to Table 11-1, “Second Generation Intel® Xeon® Scalable Processors Based Platform LGA3647-0 Socket Enabling Components” for Intel and suppliers’ part numbers.
3. PHM is Processor Heatsink Module.

Figure 9-1. Processor and Enabling Components Mechanical Assembly



Note: The processor thermal mechanical solution assembly begins with surface mounting the LGA3647-0 socket onto the baseboard. The remaining steps presumed that the socket(s) have already been surface-mounted onto the board.

Figure 9-2. LGA3647-0 Post SMT with PNP Cover



9.2 Top and Bolster Plate Installation

The first step in board or system assembly is to attach the LGA3647-0 socket and bottom plate to the motherboard. For the processor and components assembly, it is presumed that the socket(s) have already been surface-mounted onto the board. As for the bolster plate, customers may require double-sided Kapton* tape to hold the back in place for the duration of the assembly. While installing the bolster plate or placing the motherboard on the bolster plate, care should be taken to visually align them to prevent damaging the motherboard.

Note: The bolster plate must be properly oriented with respect to the motherboard. Otherwise, the processor and the top assembly will not engage properly with the motherboard and the socket.

The next step is installing the top plate with its Kapton tape pre-applied. The top plate should be placed on the motherboard while ensuring that it is properly oriented. The indicator on the top plate, as well as its holes pattern, provide clues as to its orientation. The top plate is then secured to the motherboard by attaching the large and small posts.

Warning: The large and small posts must be tightened to a maximum torque value of 0.8 N-m (7 lbf-in.). Damage to the processor and its enabling components may result if the posts are not tightened properly.

After the bolster plate is installed, the socket PNP capacitors should be carefully removed. This capacitors do prevent dust or small foreign material enter socket contact area. Hence, they should be replaced by a socket dust cover after the bolster is installed. Be sure the socket duct cover is of the correct part number for use with the installed bolster plate.

Figure 9-3. LGA3647-0 Backplate (Installed Position)

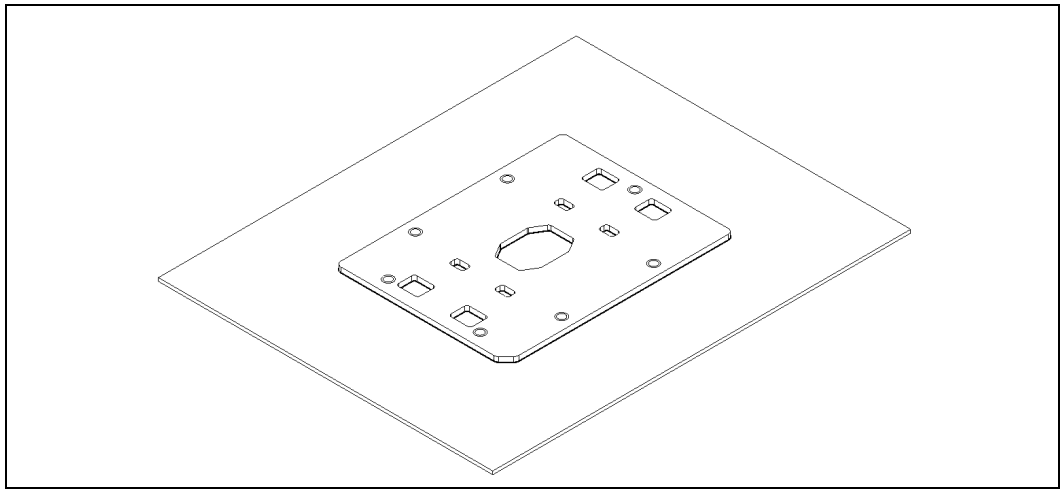
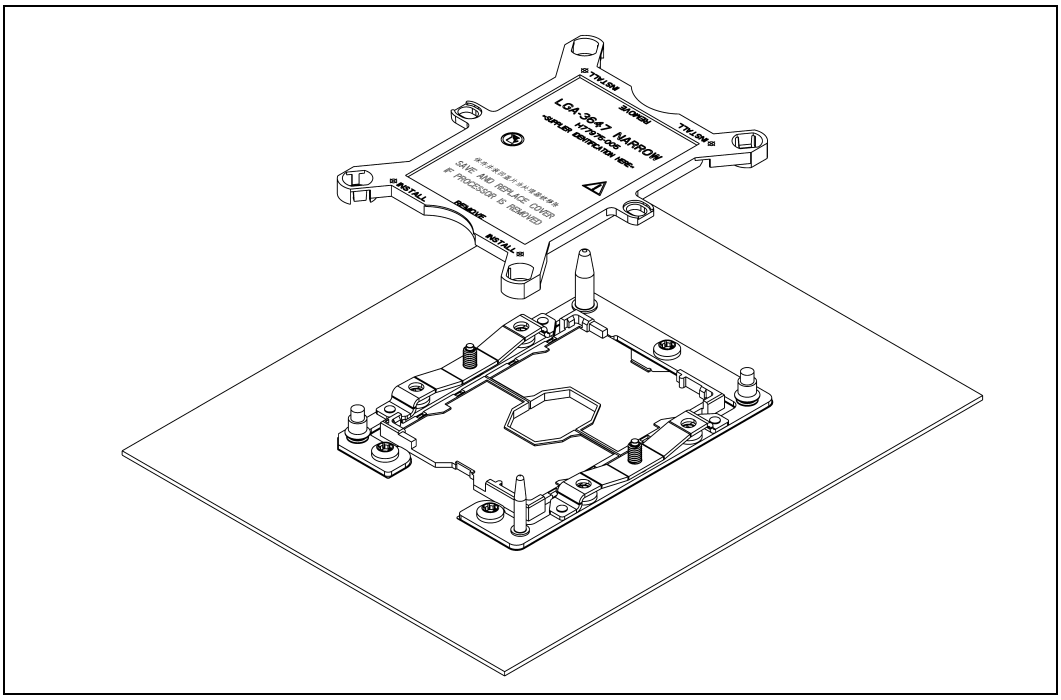


Figure 9-4. LGA3647-0 Bolster Plate in Installed Position with the Socket Dust Cover



9.3 Processor Heatsink Subassembly

Offline assembly of the processor and heatsink is done using the processor shipping tray. Assembly begins with the appropriate processor clip: orient the clip and snap it onto the processor in the tray.

Verify that the clip is fully attached to the processor before proceeding. The heatsink is next: it is assumed that the thermal interface material is already applied and remove any protective film or cover before proceeding.

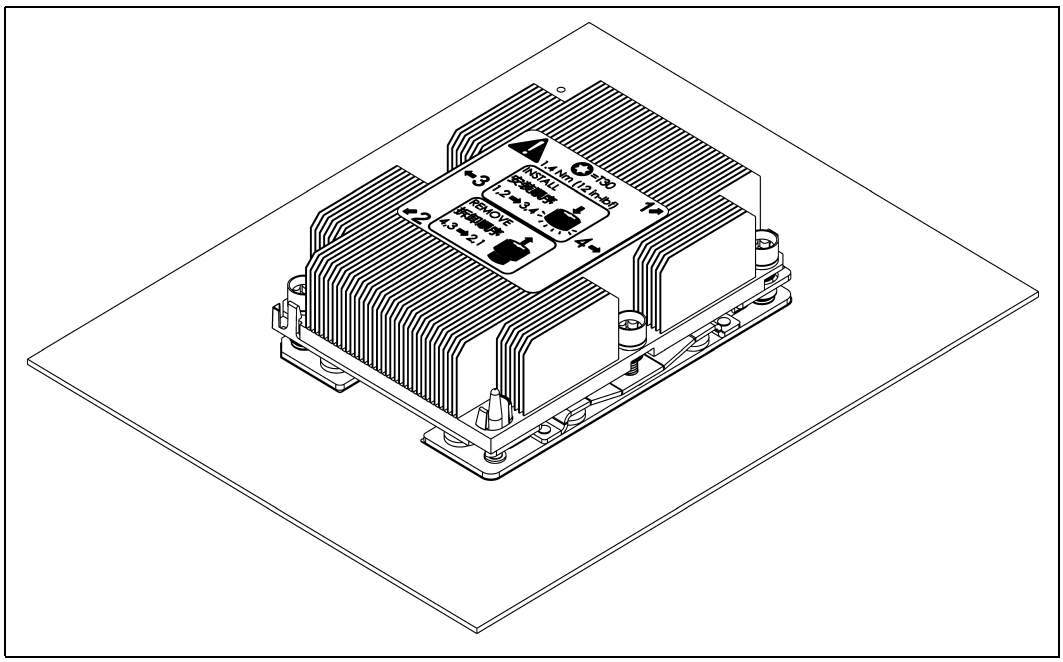
Next, properly orient the heatsink if necessary and lower it onto the processor and clip assembly from the previous step. Make sure the thermal interface material does not come in contact with any surface until it rests on the processor.

At this point, the processor clip can be snapped onto the heatsink base at the top and bottom edges and within both the oblong holes. It may be necessary to push at the top until those snap features are engaged and then at the bottom until those snap features are engaged.

Verify that all snap features of the processor clip are fully engaged before removing the PHM assembly from the tray.

Caution: If the board or the system assembly site is at a different site, then the above assembly should be properly packed to prevent any damage to the processor or the components while in transit.

Figure 9-5. Processor Heatsink Module in Installed Position



9.4 Processor Installation

Inspect the processor and heatsink assembly if they are assembled offline. The next steps assume that the board is ready for the processor installation. That is, Section 9.2 is completed.

Gently remove the socket dust cover and inspect the socket for damage or defects.

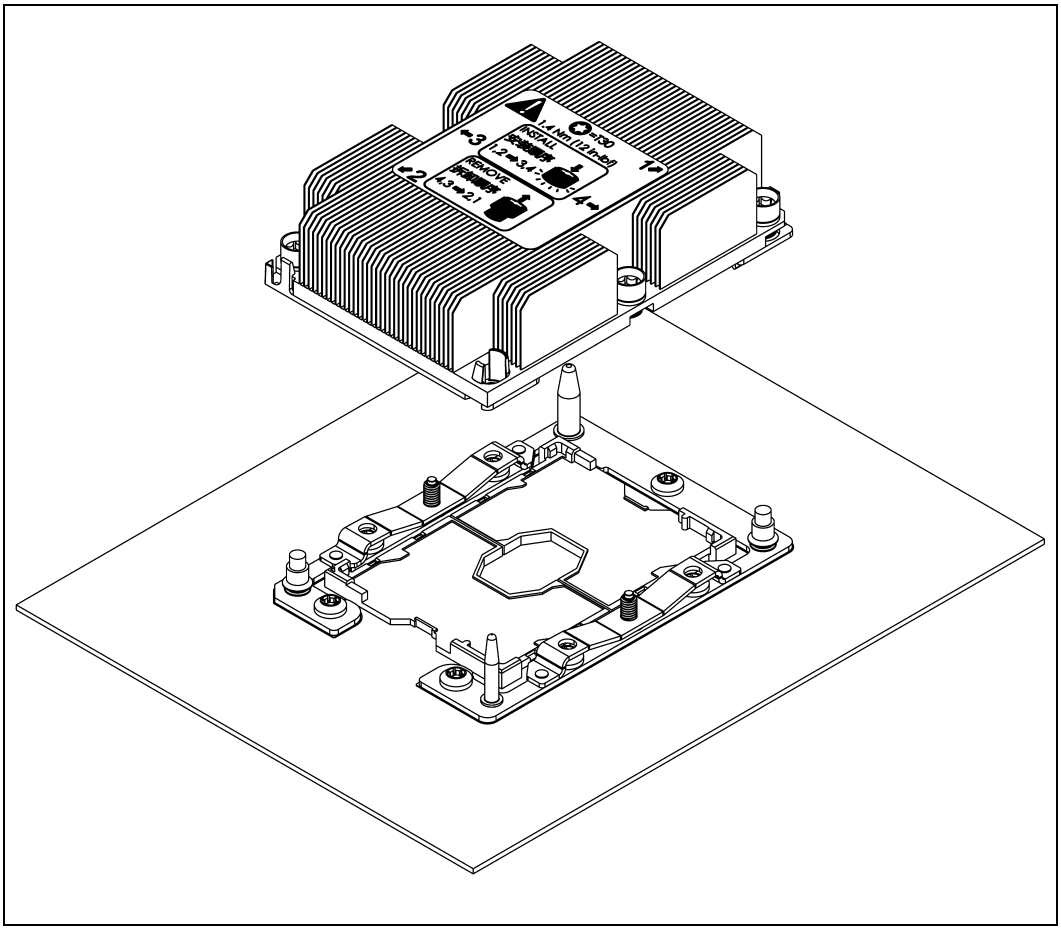
Warning: Do not install the processor if the socket contains defects.

Orient the processor assembly over the large and small posts. Gently lower the assembly, while making sure that the posts protrude through the heatsink holes.

Warning: If the processor has reached its stop but the posts are not protruded, inspect the setup to ensure processor is properly seated. This may require removing the assembly, inspecting it and the board, and reinstalling the processor assembly.

Once the processor is properly seated on the socket, tighten the corner fasteners and then tighten the spring fasteners to load the entire assembly. Be sure that all of the fasteners are tightened and inspect the assembly to ensure that it is properly installed.

Figure 9-6. LGA3647-0 Processor Heatsink Module (PHM) Ready for Installation



§

10 Reference Heatsink Design

This section describes the Intel reference heatsink design and performance specifications in accordance with the processor thermal and mechanical specifications. System form factor compatibility and thermal boundary conditions were applied in designing the heatsinks.

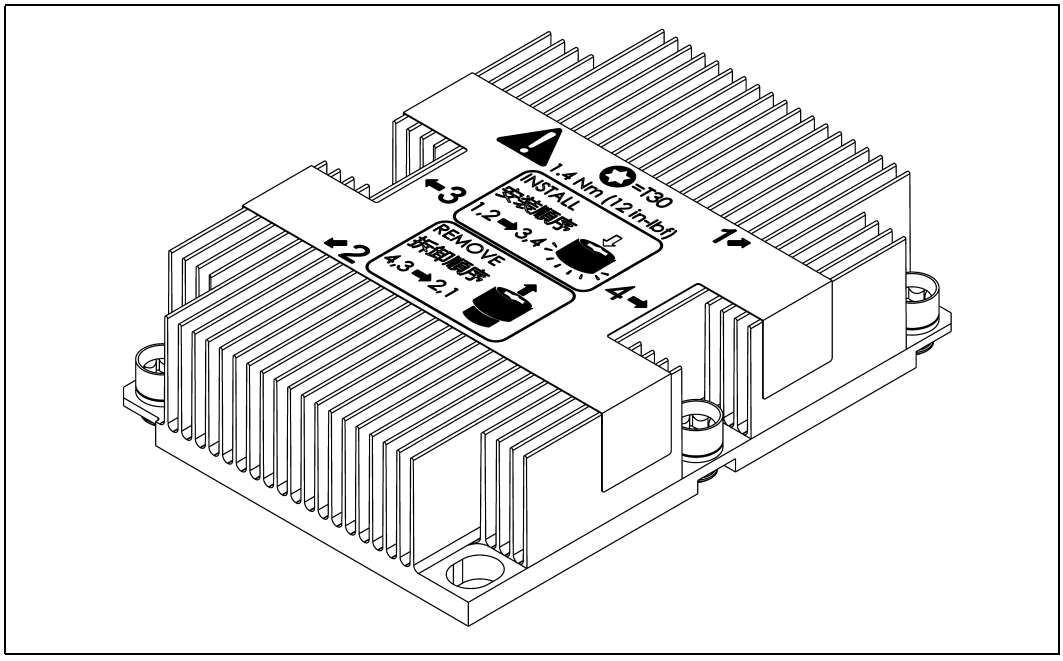
10.1 Reference Heatsink Design

Intel has several reference heat sinks for the Second Generation Intel® Xeon® Scalable Processors based platform. This section details the design targets and performance of each heatsink design within a set of environmental boundary conditions.

Table 10-1. 1U Narrow Low Impedance Heatsink

Parameter	Value
Volumetric	78 x 108 x 25.5 mm^3
Base Thickness	4.5 mm
Fin Height	21 mm
Ambient Temperature (T_{LA})	Refer to Table 5-6, "Thermal Boundary Conditions" to obtain these values.
Air Flow Rate (Q)	

Figure 10-1. 1U Narrow Low Impedance Heatsink



The next chart illustrates the heatsink performance and pressure drop as a function of the air flow rate.

Table 10-2. 1U Narrow Low Impedance Heatsink

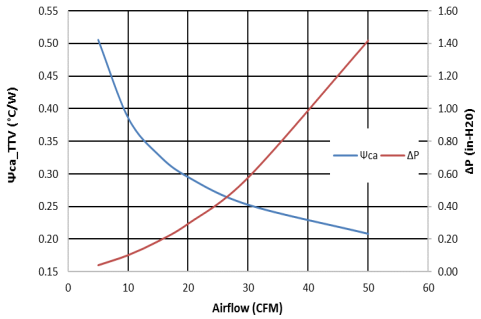
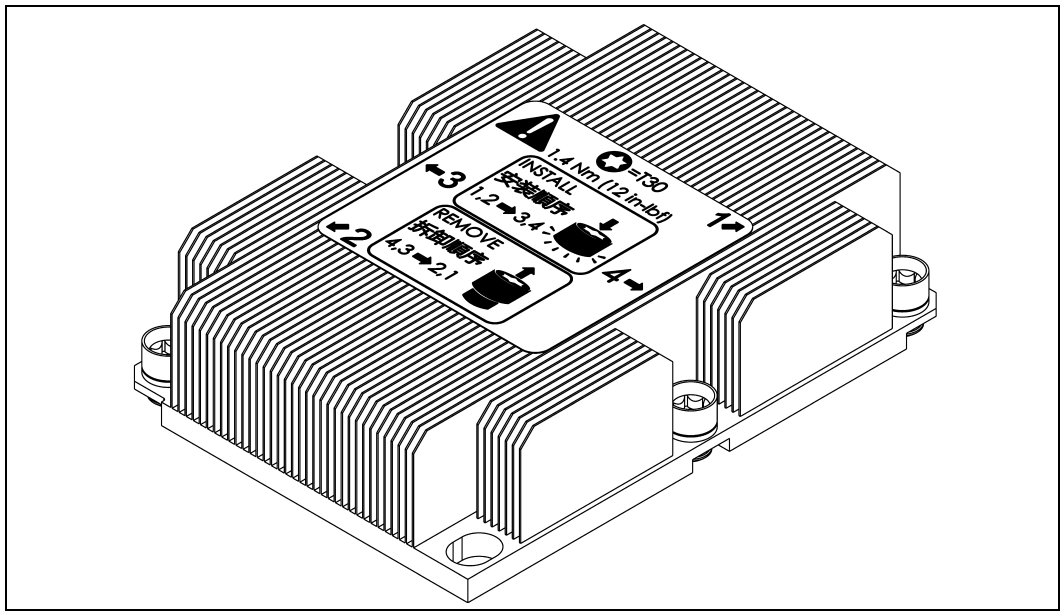
Heatsink Performance Variables	Heatsink Performance Chart
$\Psi_{CA\_TTV} = \alpha + \beta * (Q)^{-\gamma}$ α=0.014, β=0.941,γ=0.403 Q = 11.6 CFM Mean Ψ_{CA_TTV} =0.364 °C/W σ = 0.003 ΔP=4.57E-04 * Q^2 + 5.68E-03 *Q	

Table 10-3. 1U Narrow High Performance Heatsink

Parameter	Value
Volumetric	78 x 108 x 25.5 mm^3
Base Thickness	4.5 mm
Fin Height	21 mm
Ambient Temperature (T_{LA})	Refer to Table 5-6, "Thermal Boundary Conditions" to obtain these values.
Air Flow Rate (Q)	

Figure 10-2. 1U Narrow High Performance Heatsink



The next chart illustrates the heatsink performance and pressure drop as a function of the air flow rate.

Table 10-4. 1U Narrow High Performance Heatsink

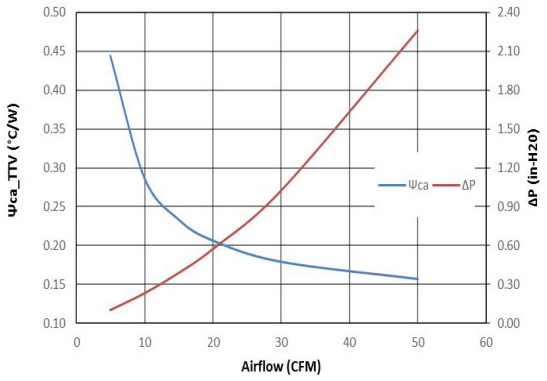
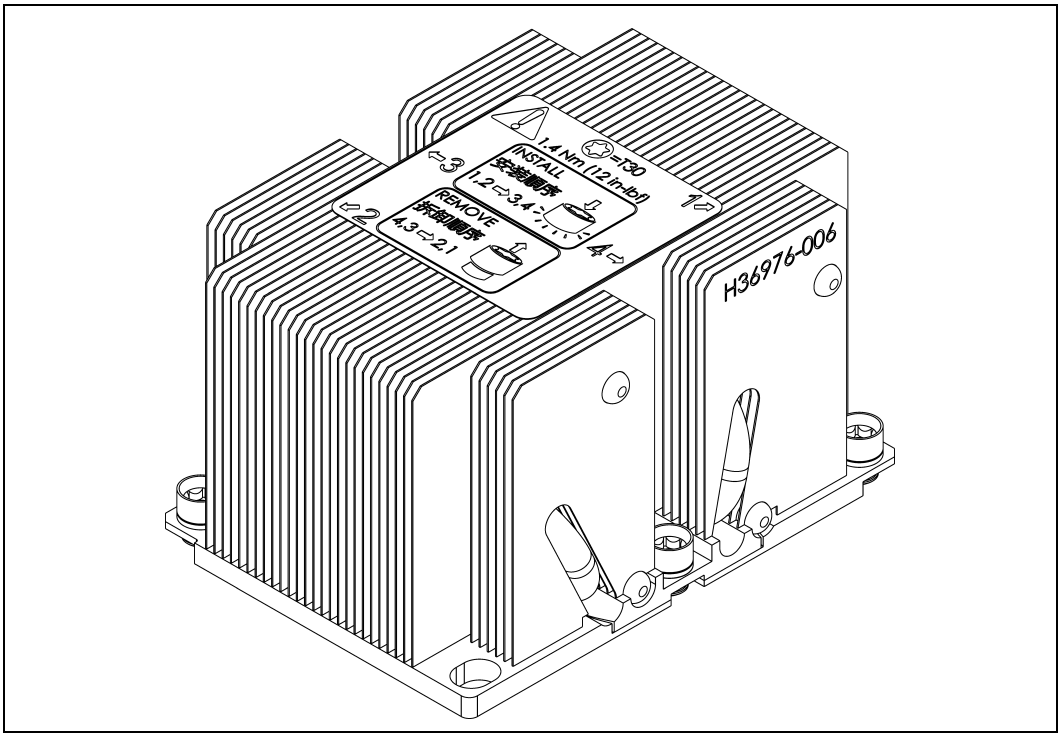
Heatsink Performance Variables	Heatsink Performance Chart
$\Psi_{CA\_TTV} = \alpha + \beta * (Q)^{-\gamma}$ α=0.122, β=1.528,γ=0.967 Q = 11.6 CFM Mean Ψ_{CA_TTV} =0.265 °C/W σ= 0.0025 ΔP=5.52E-04 * Q^2 + 1.76E-02 *Q	

Table 10-5. 2U Narrow High Performance Heat Pipe Heatsink

Parameter	Value
Volumetric	78 x 108 x 64 mm^3
Base Thickness	4.5 mm
Fin Height	59.5 mm
Heatpipe	4x with dia: 6 mm
Ambient Temperature (T_{LA})	Refer to Table 5-6, "Thermal Boundary Conditions" to obtain these values.
Air Flow Rate (Q)	

Figure 10-3. 2U Narrow High Performance Heat Pipe Heatsink



The next chart illustrates the heatsink performance and pressure drop as a function of the air flow rate.

Table 10-6. 2U Narrow High Performance Heatpipe Heatsink

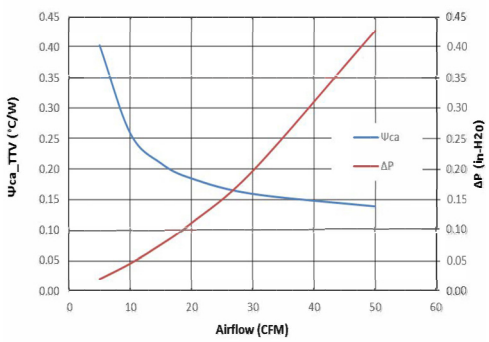
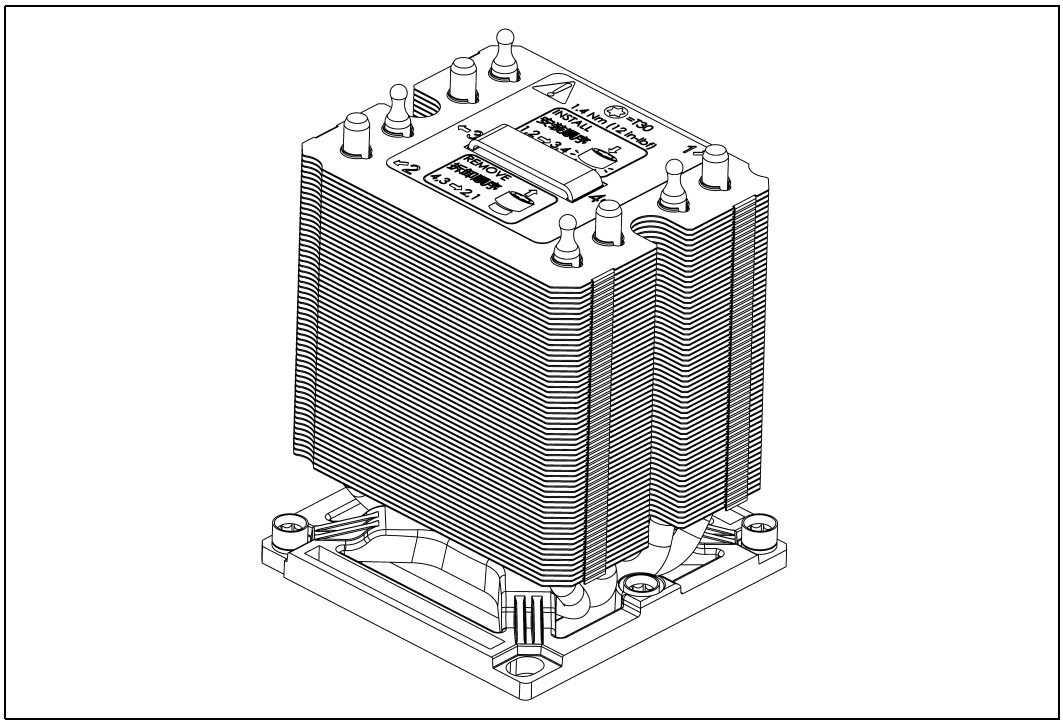
Heatsink Performance Variables	Heatsink Performance Chart
$\Psi_{CA\_TTV} = \alpha + \beta * (Q)^{-\gamma}$ α=0.106, β=1.385,γ=0.938 Q = 21.5 CFM Mean Ψ_{CA_TTV} =0.179 °C/W σ= 0.003 ΔP=9.88E-05 * Q^2 + 3.59E-03 * Q	

Table 10-7. Workstation Passive Square Heatpipe Heatsink

Parameter	Value
Volumetric	92 x 92 x 125mm^3
Base Thickness	4.5 mm
Fin Height	59.5 mm
Heatpipe	4x U shape with dia: 6 mm
Ambient Temperature (T_{LA})	Refer to Table 5-6, "Thermal Boundary Conditions" to obtain these values.
Air Flow Rate (Q)	

Figure 10-4. Workstation Passive Square Heat Pipe Heatsink



The next chart illustrates the heatsink performance and pressure drop as a function of the air flow rate.

Table 10-8. Workstation Passive Square Heatpipe Heatsink

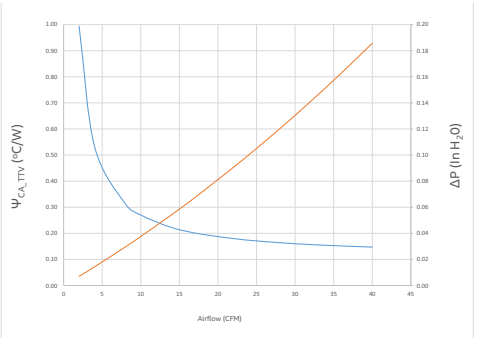
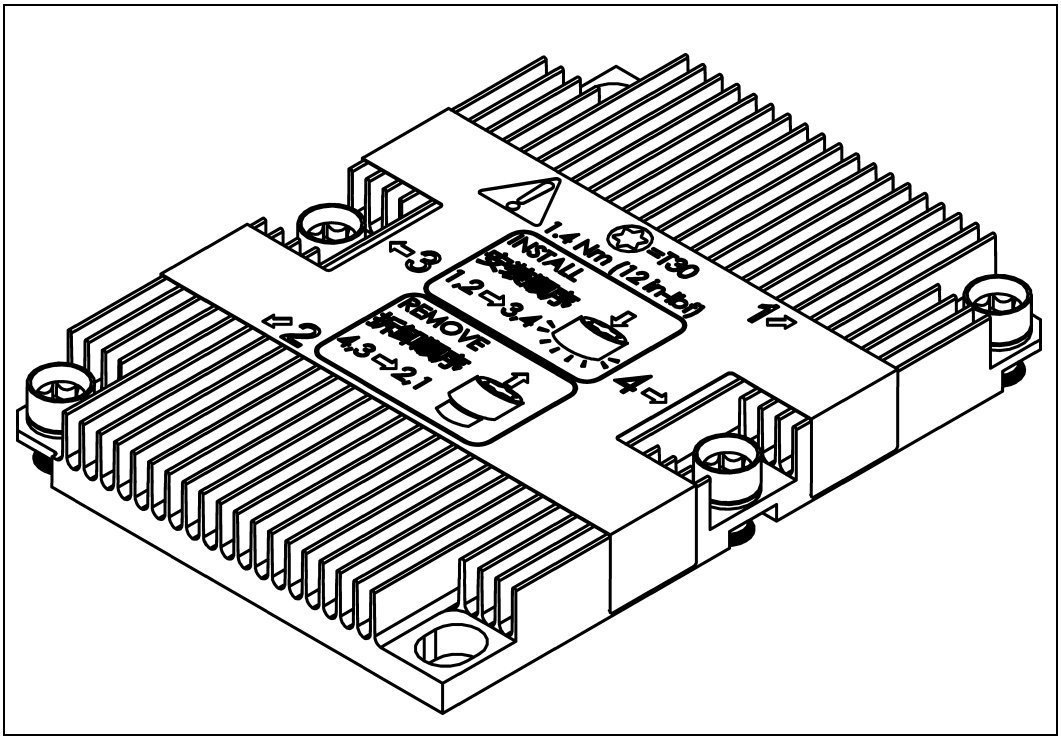
Heatsink Performance Variables	Heatsink Performance Chart
$\Psi_{CA\_TTV} = \alpha + \beta * (Q)^{-1.064}$ $\alpha = 0.111, \beta = 1.847$ Q = 23.2 CFM Mean Ψ_{CA_TTV} =0.176 °C/W σ= 0.007 ΔP=2.93E-05 * Q^2 + 3.47E-03 *Q	

Table 10-9. Non-MCP (10-Year Use + NEBS-Friendly) Low Profile Heatsink

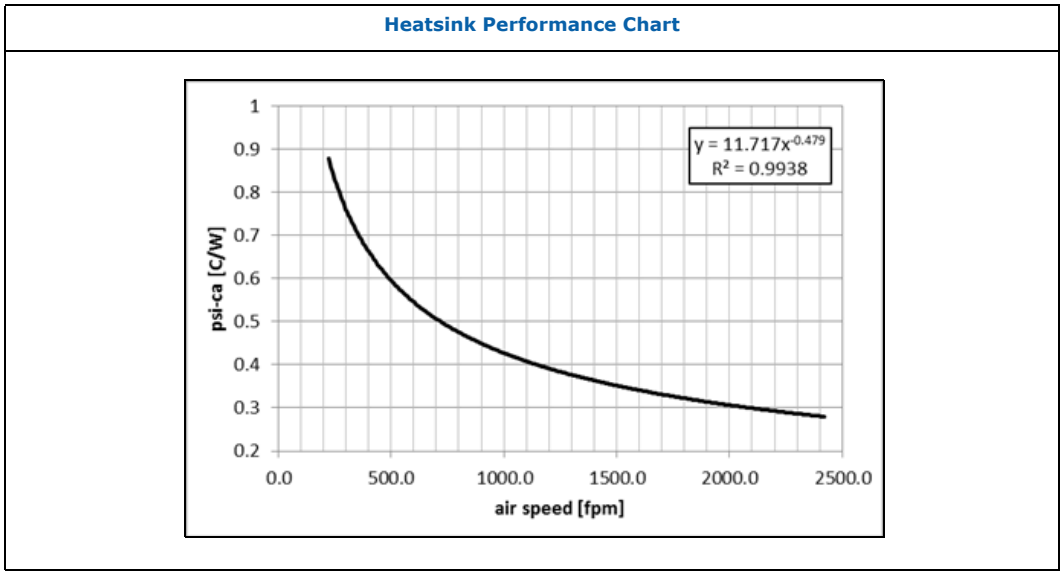
Parameter	Value
Volumetric	12.4 x 78 x 108 mm^3
Base Thickness	4.5 mm
Fin Height	7.9 mm

Figure 10-5. Non-MCP (10-Year Use + NEBS-Friendly) Low Profile Heatsink



The next figure illustrates the heatsink performance as a function of the air speed.

Figure 10-6. Non-MCP (10-Year Use + NEBS-Friendly) Low Profile Heatsink Performance Chart



10.1.1 Thermal Interface Material (TIM)

Honeywell* PCM45F pad material was chosen as the interface material for analyzing boundary conditions and processor specifications. The recommended minimum activation load for PCM45F is ~15 PSI [103 kPA]. Meeting the minimum heatsink load targets described in Table 4-1 ensures that requirement is met.

§

11 Supplier Listing

Third-party suppliers are enabled to ensure that the reference thermal and mechanical components are available.

Intel Enabled Supplier Information

Notes:

1. Supplier listing is provided by Intel as a convenience to its customers. Intel does not make any representations or warranties whatsoever regarding the quality, reliability, functionality, or compatibility of these devices.
2. All part numbers listed are in prototype phase and have not been verified to meet performance targets or quality and reliability requirements and are subject to change.
3. Supplier information provided in the table was deemed accurate when this document was released.
4. Customers must evaluate performance against their own product requirements.

Table 11-1. Second Generation Intel® Xeon® Scalable Processors Based Platform LGA3647-0 Socket Enabling Components

Component	Intel P/N	Supplier 1	Supplier 1 P/N	Supplier 2	Supplier 2 P/N	Supplier 3	Supplier 3 P/N	Note
LGA3647-0 Socket 30 µ-inch Gold Contacts (Socket P0)	J34320 - 001 Right Side Key Yellow	Tyco Electronics Connectivity* (TE)	2-2129710-6	NA	NA	NA	NA	3
	J34320 - 002 Left Side Key Black	Tyco Electronics Connectivity (TE)	2-2129710-5	NA	NA	NA	NA	3
	J34318 - 001 Right Side Key Yellow	NA	NA	Foxconn Interconnect Technology*	PE36473-01NK3-1H	NA	NA	3
	J34318 - 002 Left Side Key Black	NA	NA	Foxconn Interconnect Technology	PE36473-01NK4-1H	NA	NA	3
	Right Side Key Yellow	NA	NA	NA	NA	LOTES CO LTD	AZIFS007-P002C01	3
	Left Side Key Black	NA	NA	NA	NA	LOTES CO LTD	AZIFS008-P002C01	3
LGA3647-0 Socket 15 µ-inch Gold Contacts (Socket P0)	J65187 - 001 Right Side Key Yellow	Tyco Electronics Connectivity (TE)	2-2129710-2	NA	NA	NA	NA	3
	J65187 - 002 Left Side Key Black	Tyco Electronics Connectivity (TE)	2-2129710-1	NA	NA	NA	NA	3
	H37603 - 202 Right Side Key Yellow	NA	NA	Foxconn Interconnect Technology	PE36477-01NK1-1H	NA	NA	3
	H37603 - 203 Left Side Key Black	NA	NA	Foxconn Interconnect Technology	PE36477-01NK2-1H	NA	NA	3
	Right Side Key Yellow	NA	NA	NA	NA	LOTES CO LTD	AZIFS007-P001C01	3
	Left Side Key Black	NA	NA	NA	NA	LOTES CO LTD	AZIFS008-P001C01	3

Table 11-1. Second Generation Intel® Xeon® Scalable Processors Based Platform LGA3647-0 Socket Enabling Components

Component	Intel P/N	Supplier 1	Supplier 1 P/N	Supplier 2	Supplier 2 P/N	Supplier 3	Supplier 3 P/N	Note
Socket-P Heatsink Nut Collar	H94875-004	KYZ	A10360H	NA	NA	NA	NA	3
Socket-P Delrin* Heatsink Washer	H37265-004	KYZ	A10247H	ITW	FT1604-A	NA	NA	3
Socket-P Intel® Xeon® Processor Scalable Processors Heatsink Nut	H98449-003	ITW	FT1614-A	NA	NA	NA	NA	3
Thermal Interface Material PCM45F 70X47X0.25 mm	H38442-001	Honeywell International, Inc.*	099079	NA	NA	NA	NA	3
Narrow Fabric PHLM								
Narrow Fabric Bolster Plate	H95384-004	LOTES CO LTD*	AZIF0087-P002C*	Foxconn Interconnect Technology	WNMEL60-80N04-EH	Tyco Electronics Connectivity (TE)	2310924-3	3
Narrow Socket Dust Cover	H77975-005	LOTES CO LTD	AZIF0084-P002C*	Foxconn Interconnect Technology	WNMEL00-81N00-EH	Tyco Electronics Connectivity (TE)	2305234-1	3
Narrow Fabric Bolster and Socket Dust Cover	NA	LOTES CO LTD	AZIF0088-P002C*	Foxconn Interconnect Technology	PT44L11-4811	Tyco Electronics Connectivity (TE)	2310924-1	3
Narrow Fabric Bolster with Dust Cover and Backplate	NA	LOTES CO LTD	AZIF0112-P002C*	Foxconn Interconnect Technology	WNMEA66-81N01-EH	Tyco Electronics Connectivity (TE)	2314678-3	3
Narrow Non-Fabric PHLM								
Narrow Backplate (board thickness 1.6 - 2.36 mm (0.063" - 0.093")	H77928-002	LOTES CO LTD	AHSK0010-P003C*	Foxconn Interconnect Technology	PT44P11-4801	Tyco Electronics Connectivity (TE)	2299805-1	3
Narrow Backplate (board thickness 2.36 - 3.3 mm (0.093" - 0.130")	J36227-001	LOTES CO LTD	AHSK0013-P003C*	Foxconn Interconnect Technology	WNMEP06-80600-EH	Tyco Electronics Connectivity (TE)	2299805-3	3
Narrow non-fabric Bolster Plate	H95385-004	LOTES CO LTD	AZIF0089-P002C*	Foxconn Interconnect Technology	WNMEL60-80N03-EH	Tyco Electronics Connectivity (TE)	2299804-3	3
Narrow Socket Dust Cover	H77975-005	LOTES CO LTD	AZIF0084-P002C*	Foxconn Interconnect Technology	WNMEL00-81N00-EH	Tyco Electronics Connectivity (TE)	2305234-1	3

Table 11-1. Second Generation Intel® Xeon® Scalable Processors Based Platform LGA3647-0 Socket Enabling Components

Component	Intel P/N	Supplier 1	Supplier 1 P/N	Supplier 2	Supplier 2 P/N	Supplier 3	Supplier 3 P/N	Note
Narrow non-Fabric Bolster and Socket Dust Cover	NA	LOTES CO LTD	AZIF0090-P002C*	Foxconn Interconnect Technology	WNMEL60-80N00-EH	Tyco Electronics Connectivity (TE)	2299804-1	3
Narrow non-Fabric Package Carrier	H72851-002	LOTES CO LTD	AZIF0081-P002C*	Foxconn Interconnect Technology	WNMEL00-82N00-EH	Tyco Electronics Connectivity (TE)	2299806-1	3
Narrow non-Fabric Bolster with Dust Cover and Backplate	NA	LOTES CO LTD	AZIF0113-P002C*	Foxconn Interconnect Technology	WNMEA66-81N00-EH	Tyco Electronics Connectivity (TE)	2314678-1	3
Heatsinks								
1U High Performance Heatsink	H38569-008	Foxconn Technology Co. Ltd	1A21BJ900-RPC	NA	NA	NA	NA	3
1U Low Impedance Heatsink	H45651-006	CCI	0A14092601	Foxconn Technology Co. Ltd	1A21MPL00	NA	NA	3
2U Narrow Heatsink (Compatible with 2U and 4U system form factors)	H36976-007	Foxconn Technology Co. Ltd	1A21BMU00-RPC	NA	NA	NA	NA	3
Non-MCP (10-Year Use + NEBS-Friendly) Low Profile Heatsink	J12672-003	CCI	0A15386301	NA	NA	NA	NA	3

Notes:
1. See the component specifications for detail and ordering information.
2. Contact the local Intel representative for sample availability.
3. Components part numbers are subject to change. Contact your Intel representative and the suppliers for the latest revisions, compatibility between revisions, and availability schedule.

Table 11-2. Components Supplier Contact Listing

ID	Supplier	Contact
1	Lotes Co LTD*	Cathy Yang Tel. +1-86-20-8468 6519 email: Cathy@lotes.com.cn
2	Foxconn Technology Co LTD*	Ray Wang Tel. +1 512 351-1493 x273 email: ray.wang@foxconn.com
3	Molex Inc*	Joe Dambach Tel. +1 630-527-4546 email: Joe.Dambach@molex.com
4	Tyco Electronics Corporation (TE)*	Ellen Liang Tel. +886 2 2171 5261 email: ellen.yh.liang@te.com
5	Foxconn Interconnect Technology (FIT)*	Eric Ling Tel. +1 971-506-6441 +1 503-327-8346 email: eric.ling@fit-foxconn.com
6	CCI (Chaun-Choung) Technology Corp.*	12F,No 123-1, Hsing-De Rd., Sanchung, Taipei, Taiwan, R.O.C. Tel. +886 (2) 2995-2666 x1131 Fax: +886 (2) 2995-8258 Monica Chih Monica_chih@ccic.com.tw Sean Wu sean_wu@ccic.com.tw (408)429-4670
7	Honeywell International, Inc.*	430 Li Bing Rd, Zhangjiang Hi-Tech Park, Pudong, Shanghai, China. Connie Smiriglio (Account Manager) Tel. +1 845-627-2750 email: Connie.smiriglio@honeywell.com Hyo Xi (Technical) Tel. 8621-28943106
8	KYZ	No.8, Xinhe Rd., Zhang Pu Town, Kunshan City, Jiangsu Province, China TW Tel: 02-82005703 CH Tel: 051257293826 Gary Yuan Tel. + 886 987237801 email: gary_yuan@kyz.com.tw Anna Luo Tel. +886 981006216 email: anna_luo@kyz.com.tw
9	ITW EBA	Chak Chakir Tel. 512.989.7771 email: chak.chakir@itweba.com

§

A Quality and Reliability Requirements

A.1 Thermal/Mechanical Solution Stress Test

Intel evaluates reliability performance based on the use conditions (operating environment) of the end product by using acceleration models.

The use condition environment definitions provided in the next tables are based on speculative use condition assumptions, and are provided as examples only.

Based on the system enabling boundary condition, the solder ball temperature can vary and needs to be comprehended for reliability assessment.

Table A-1. Thermal Stress Test Examples

Use Environment	Speculative Stress Condition	Example Use Condition	Example 7 yr. Stress Equivalent	Example 10 yr. Stress Equivalent
Slow small internal gradient changes due to external ambient (temperature cycle or externally heated) Fast, large gradient on/off to max operating temp. (power cycle or internally heated including power save features)	Temperature Cycle	D T = 35 - 44 °C (solder joint)	550-930 cycles Temp Cycle (-25 °C to 100 °C)	780-1345 cycles Temp Cycle (-25 °C to 100 °C)
High ambient moisture during low-power state (operating voltage)	THB/HAST	T = 25 -30 °C 85%RH (ambient)	110-220 hrs at 110 °C 85% RH	145-240 hrs at 110 °C 85% RH
High operating temperature and short duration high temperature exposures	Bake	T = 95 - 105 °C (contact)	700 - 2500 hrs at 125 °C	800 - 3300 hrs at 125 °C

Table A-2. Mechanical Stress Test Examples

Use Environment	Speculative Stress Condition		Example Use Condition
Shipping and Handling	Mechanical Shock System-level Unpackaged Trapezoidal • 25 g Velocity change is based on packaged weight		Total of 12 drops per system: 2 drops per axis ± direction
	Product Weight (lbs)	Non-palatalize Product	
	< 20 lbs	Velocity Change (in/sec)	
	20 to > 40	250	
	40 to > 80	225	
	80 to < 100	205	
	100 to < 120	175	
	≥120	145	
		125	
	Change in velocity is based upon a 0.5 coefficient of restitution.		
Shipping and Handling	Random Vibration System Level Unpackaged 5 Hz to 500 Hz 2.20 g RMS random • 5 Hz at 0.001 g^2/Hz to 20 Hz at 0.01 g^2/Hz (slope up) 20 Hz to 500 Hz at 0.01 g^2/Hz (flat) Random control limit tolerance is ± 3 dB	Total per system: 10 minutes per axis 3 axes	

A.2 Intel Reference Component Validation

Intel tests reference components individually and as an assembly on mechanical test boards and assesses performance to the envelopes specified in previous sections by varying boundary conditions.

While component validation shows a reference design is tenable for a limited range of conditions, customers need to assess their specific boundary conditions and perform reliability testing based on their use conditions.

Intel reference components are also used in board functional tests to assess performance for specific conditions.

A.3 Ecological Requirement

Material should be resistant to fungal growth. Examples of non-resistant materials include cellulose materials, animal and vegetable based adhesives, grease, oils, and many hydrocarbons. Synthetic materials such as PVC formulations, certain polyurethane compositions (for example, polyester and some polyethers), plastics which contain organic fillers of laminating materials, paints, and varnishes also are susceptible to fungal growth. If materials are not fungal growth resistant, then MIL-STD-810E, Method 508.4 must be performed to determine material performance.

Cadmium should not be used in the painting or plating of the socket. CFCs and HFCs should not be used in manufacturing the socket.

Any plastic component exceeding 25 gm should be recyclable per the European Blue Angel recycling standards.

Supplier is responsible for complying with industry standards regarding environmental care as well as with the specific standards required per the supplier's region. More specifically, the supplier is responsible for compliance with the European regulations related to restrictions on the use of lead and bromine containing flame-retardants.

Legislation varies by geography, European Union (RoHS/WEEE), China, California, and so forth.

The following definitions apply to the use of the terms lead-free, Pb-free, and RoHS compliant.

Halogen flame retardant free (HFR-Free) PCB: Current guidance for the socket pad layout supports FR4 and HFR-free designs. In future revisions of this document, Intel will be providing guidance on the mechanical impact to using a HFR-free laminate in the PCB. This will be limited to workstations.

Lead-free and Pb-free: Lead has not been intentionally added, but lead may still exist as an impurity below 1000 ppm.

RoHS compliant: Lead and other materials banned in the RoHS directive are either (1) below all applicable substance thresholds as proposed by the EU or (2) an approved/ pending exemption applies.

Note: RoHS implementation details are not fully defined and may change.

§

B Processor Package Mechanical Drawings

Table B-1 lists the processor Package Mechanical Drawings (PMD) included in this chapter.

Table B-1. Processor Package Drawing List

Drawing Description	Figure Number
PMD XCC: Non-Fabric Form Factor	Figure B-1
PMD HCC Form Factor	Figure B-2
PMD LCC Form Factor	Figure B-3

Figure B-1. PMD XCC: Non-Fabric Form Factor (Sheet 1 of 3)

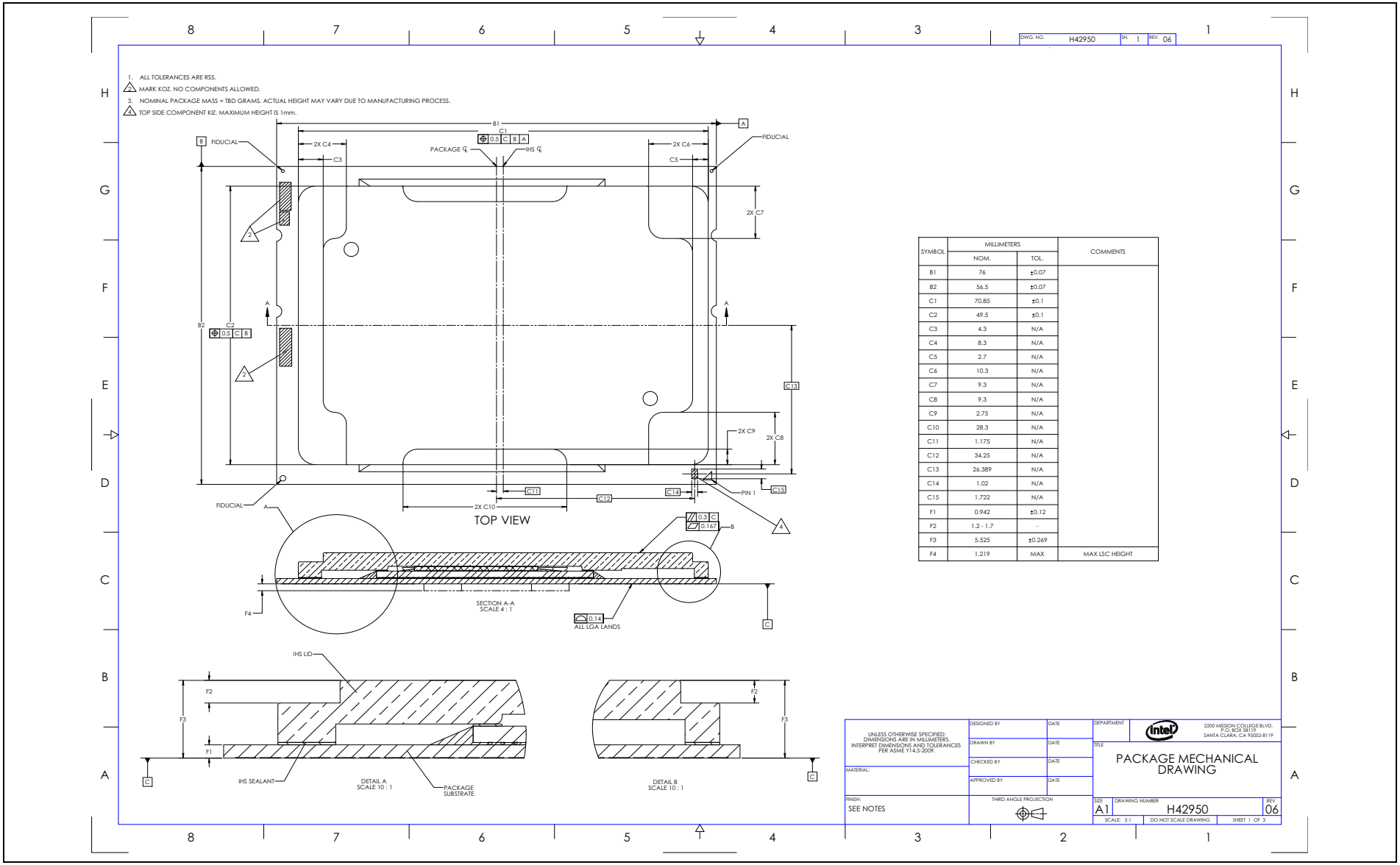
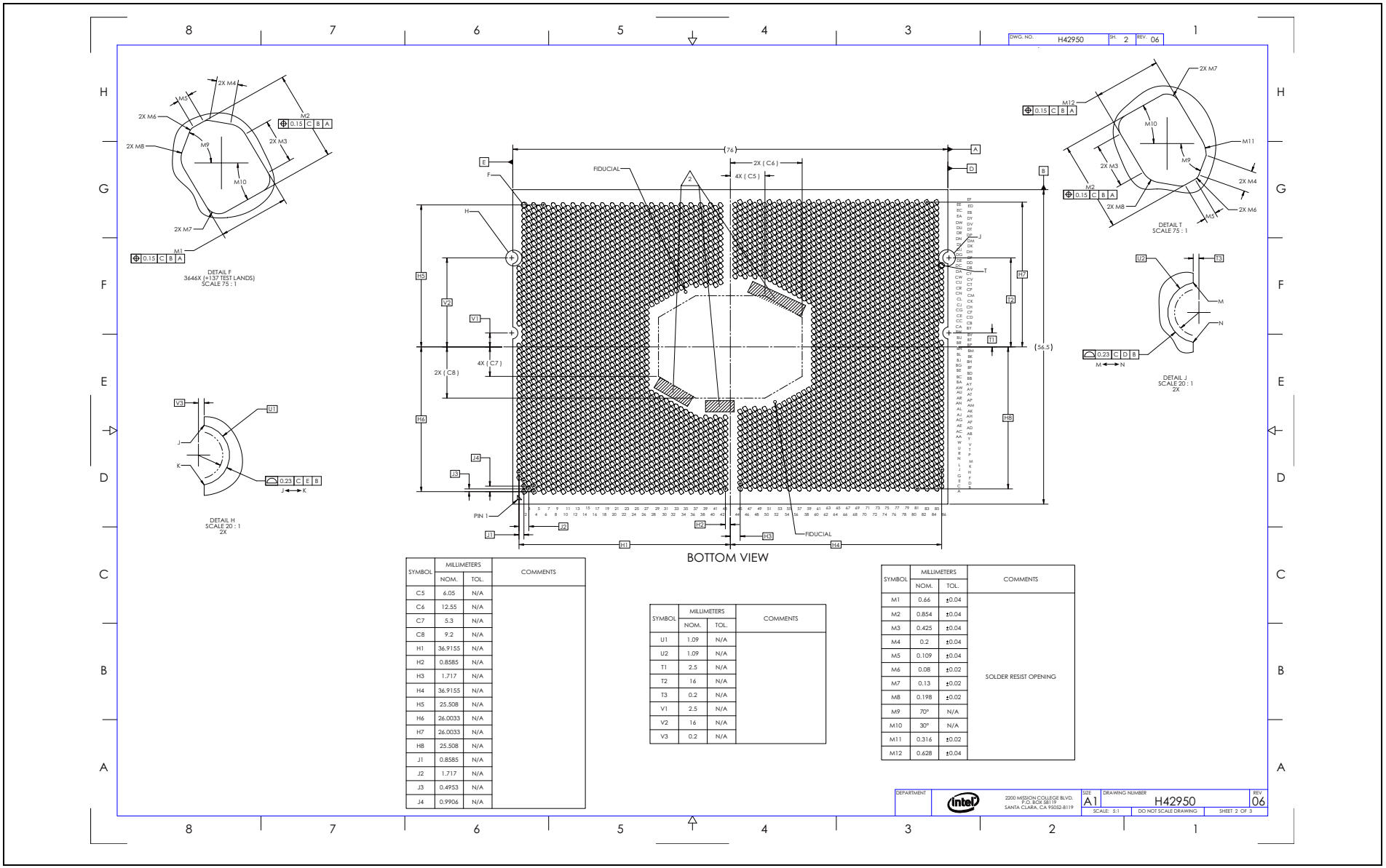


Figure B-1. PMD XCC: Non-Fabric Form Factor (Sheet 2 of 3)



SYMBOL	MILLIMETERS NOM.	MILLIMETERS TOL.	COMMENTS
C5	6.05	N/A	
C6	12.55	N/A	
C7	5.3	N/A	
C8	9.2	N/A	
H1	36.9155	N/A	
H2	0.8585	N/A	
H3	1.717	N/A	
H4	36.9155	N/A	
H5	25.508	N/A	
H6	26.0033	N/A	
H7	26.0033	N/A	
H8	25.508	N/A	
J1	0.8585	N/A	
J2	1.717	N/A	
J3	0.4953	N/A	
J4	0.9906	N/A	

SYMBOL	MILLIMETERS NOM.	MILLIMETERS TOL.	COMMENTS
U1	1.09	N/A	
U2	1.09	N/A	
T1	2.5	N/A	
T2	16	N/A	
T3	0.2	N/A	
V1	2.5	N/A	
V2	16	N/A	
V3	0.2	N/A	

SYMBOL	MILLIMETERS NOM.	MILLIMETERS TOL.	COMMENTS
M1	0.66	±0.04	
M2	0.854	±0.04	
M3	0.425	±0.04	
M4	0.2	±0.04	
M5	0.109	±0.04	
M6	0.08	±0.02	
M7	0.13	±0.02	
M8	0.198	±0.02	
M9	70°	N/A	
M10	30°	N/A	
M11	0.316	±0.02	
M12	0.628	±0.04	

Figure B-1. PMD XCC: Non-Fabric Form Factor (Sheet 3 of 3)

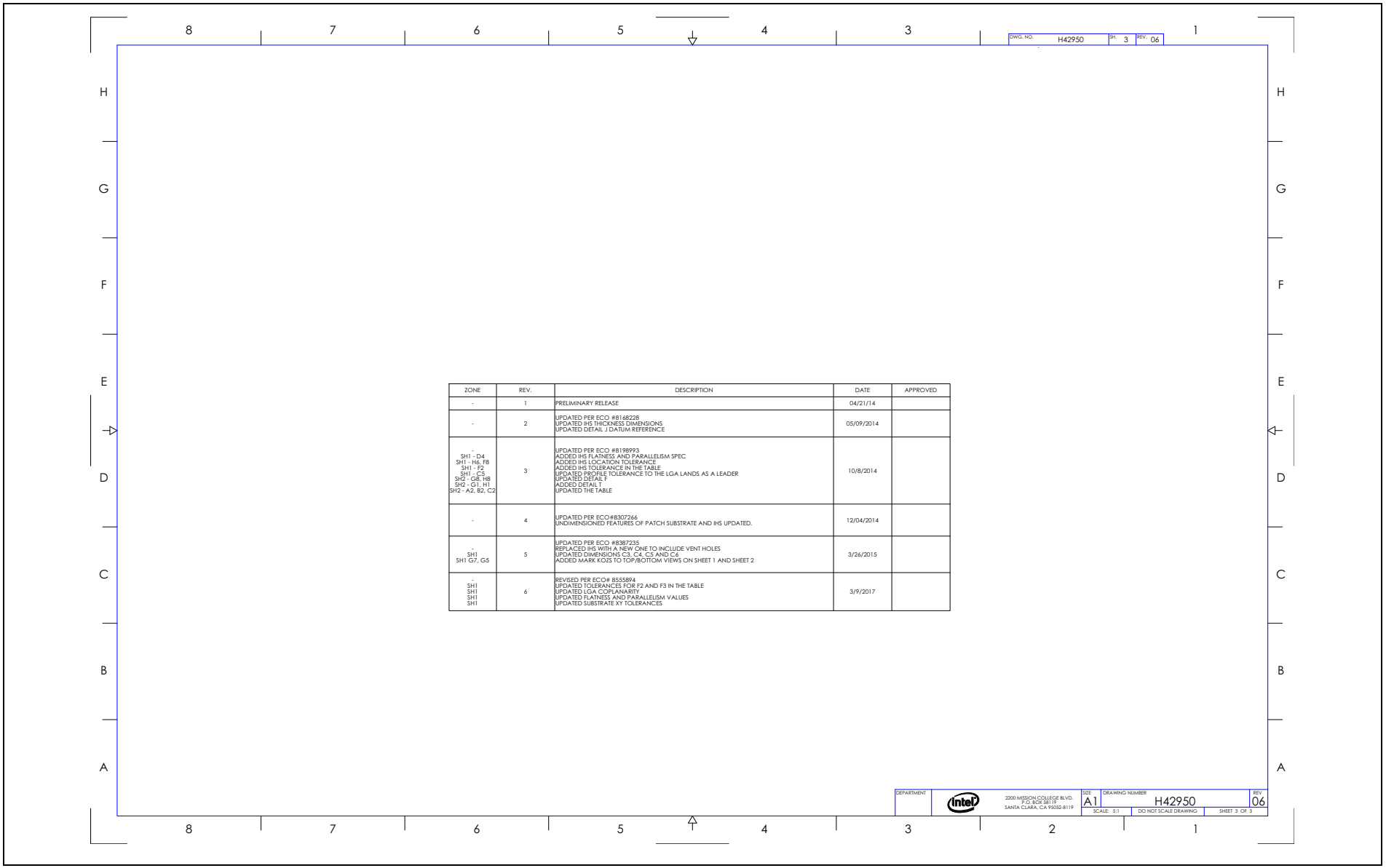


Figure B-2. PMD HCC Form Factor (Sheet 1 of 3)

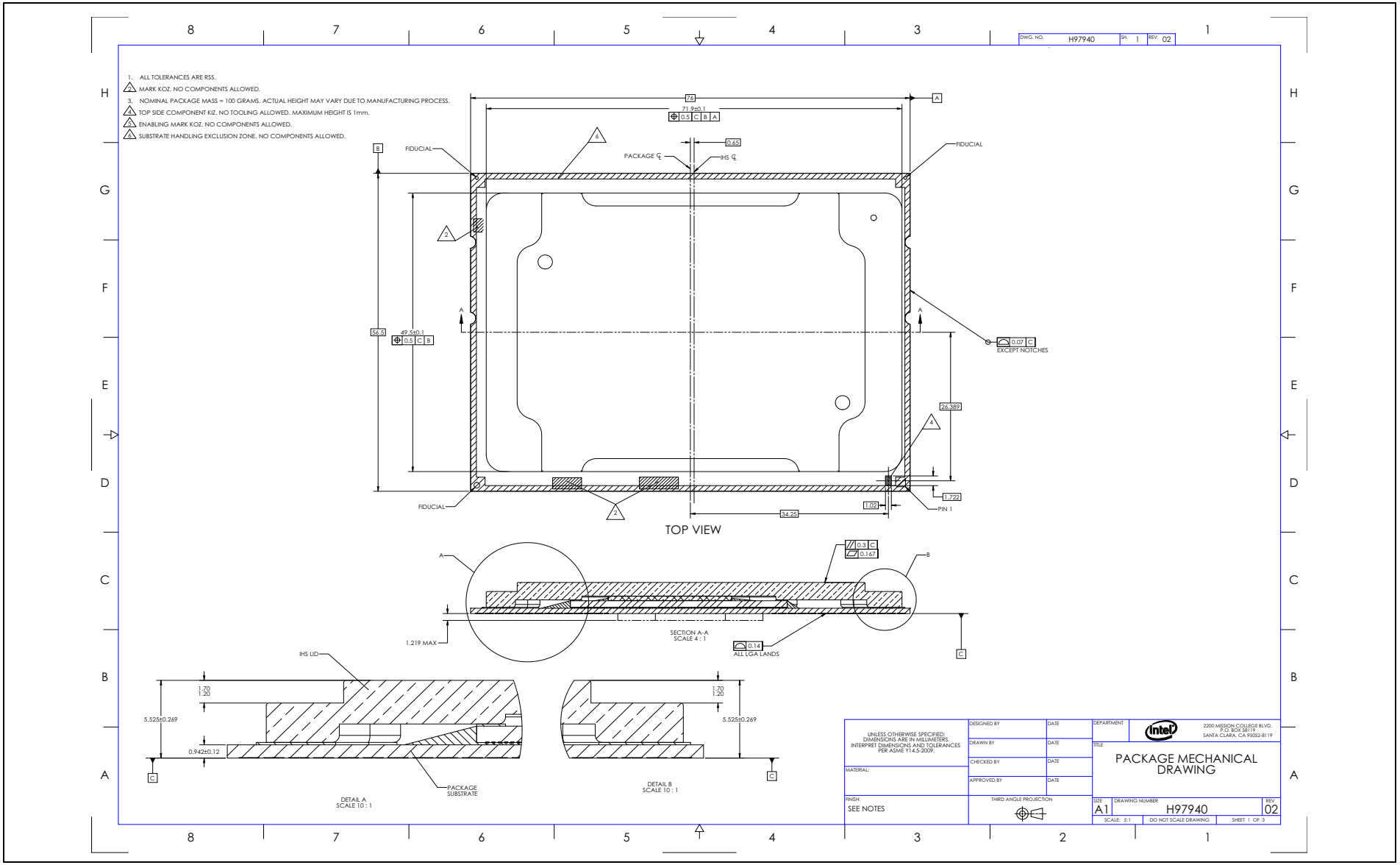


Figure B-2. PMD HCC Form Factor (Sheet 2 of 3)

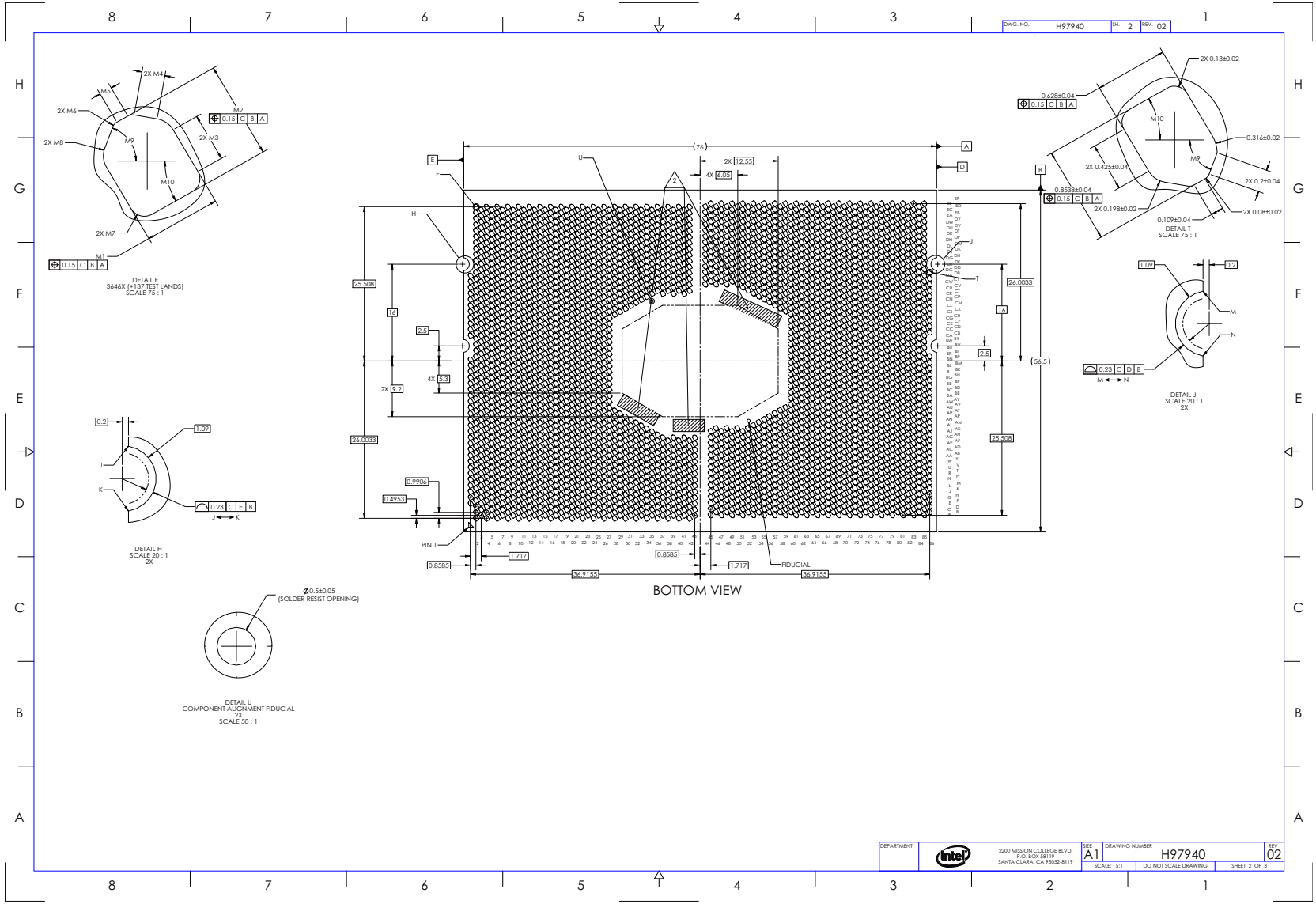


Figure B-2. PMD HCC Form Factor (Sheet 3 of 3)

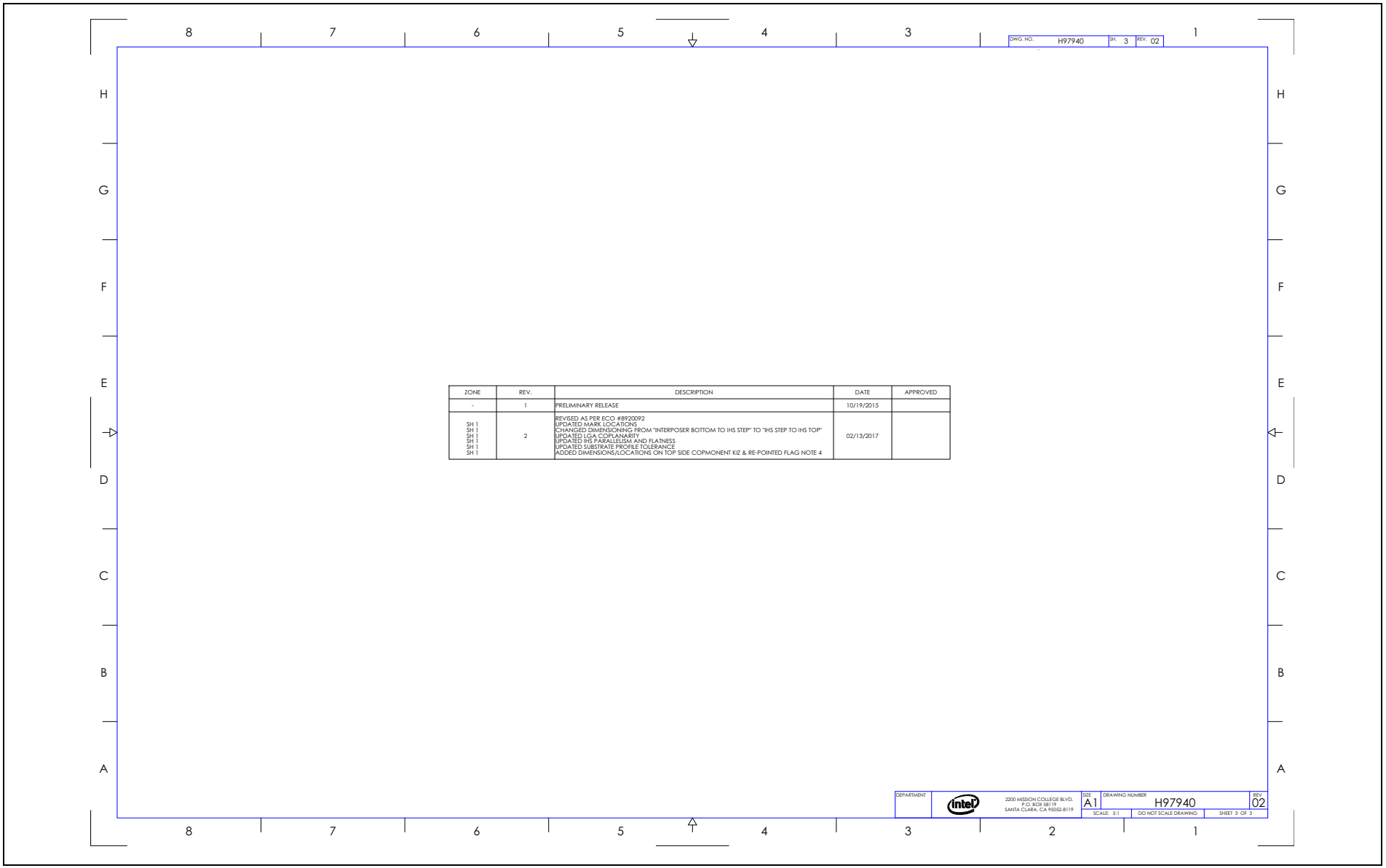


Figure B-3. PMD LCC Form Factor (Sheet 1 of 3)

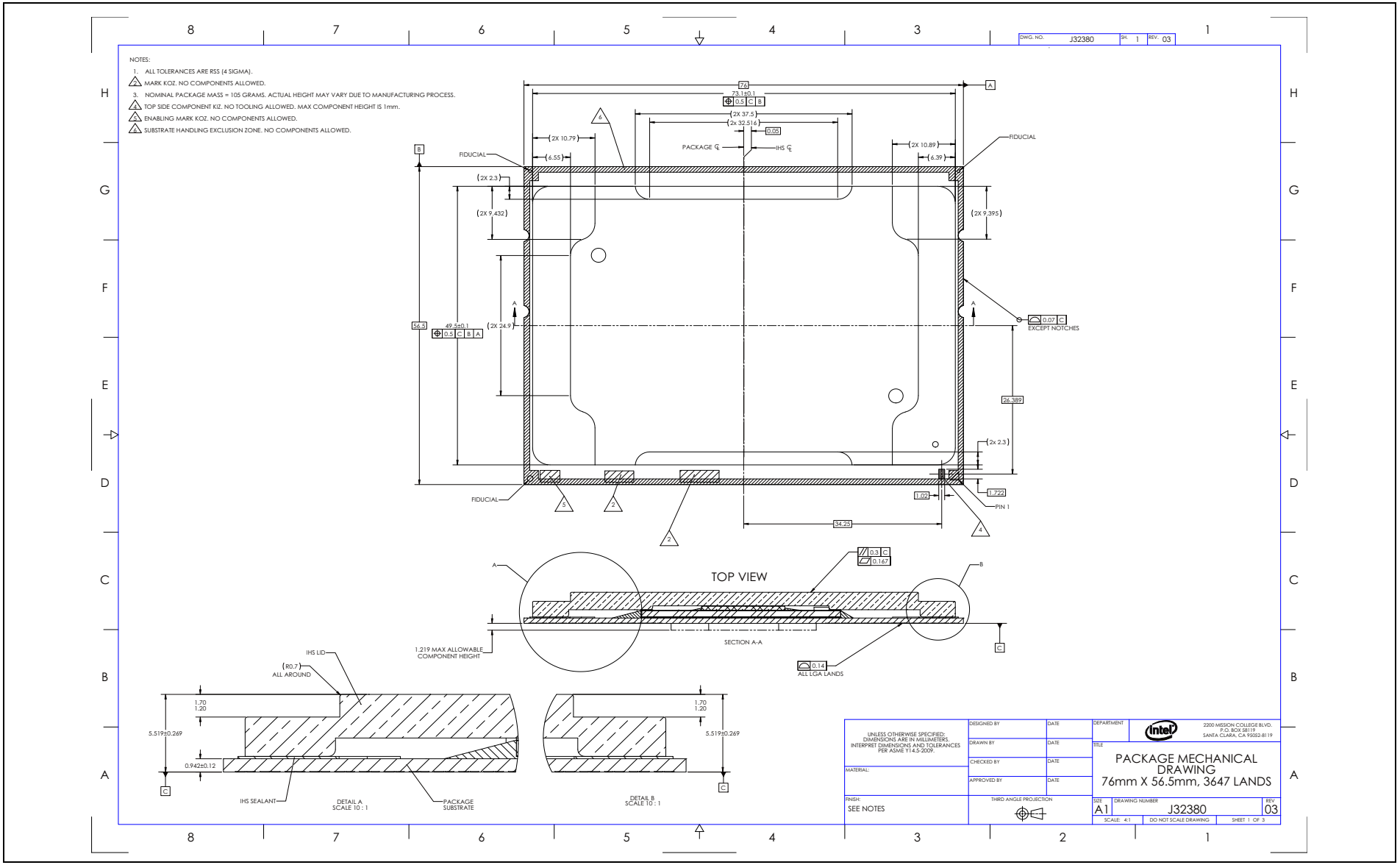


Figure B-3. PMD LCC Form Factor (Sheet 2 of 3)

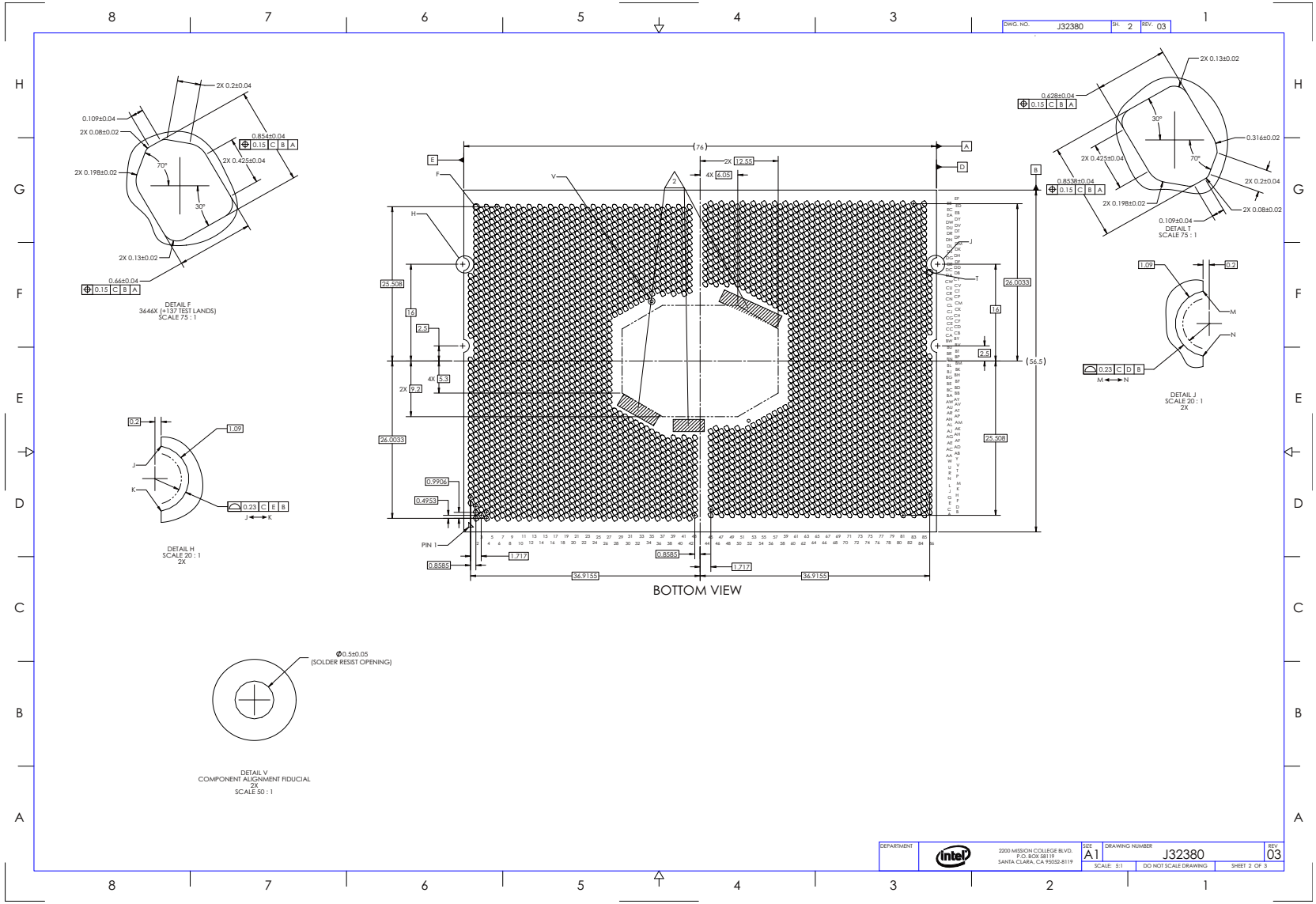
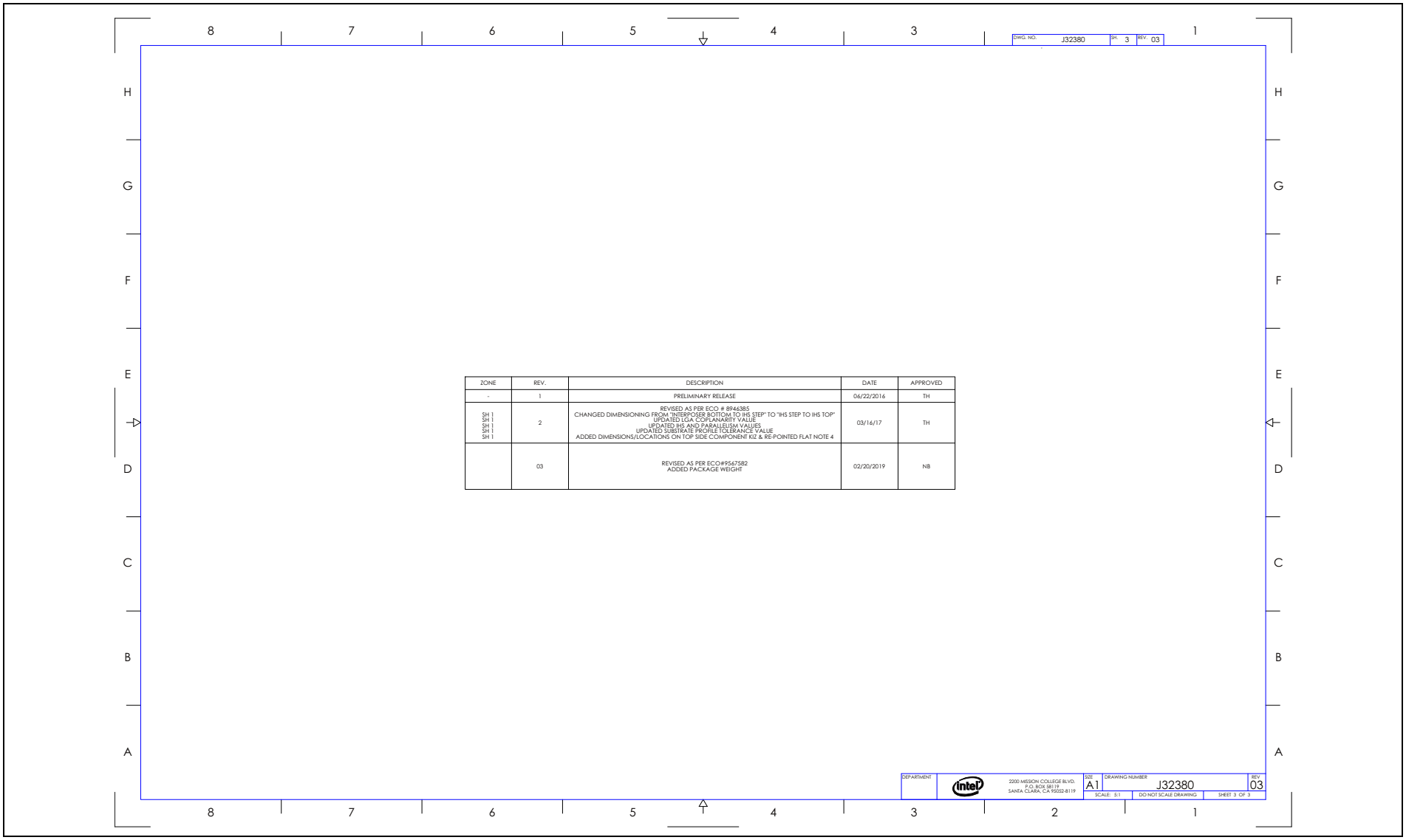


Figure B-3. PMD LCC Form Factor (Sheet 3 of 3)



§

C LGA3647-0 Socket-P0 Mechanical Drawings

Table C-1 lists the socket drawings included in this chapter.

Table C-1. Socket Drawing List

Drawing Description	Figure Number
Socket Mechanical Drawing	Figure C-1

Figure C-1. Socket Mechanical Drawing (Sheet 1 of 4)

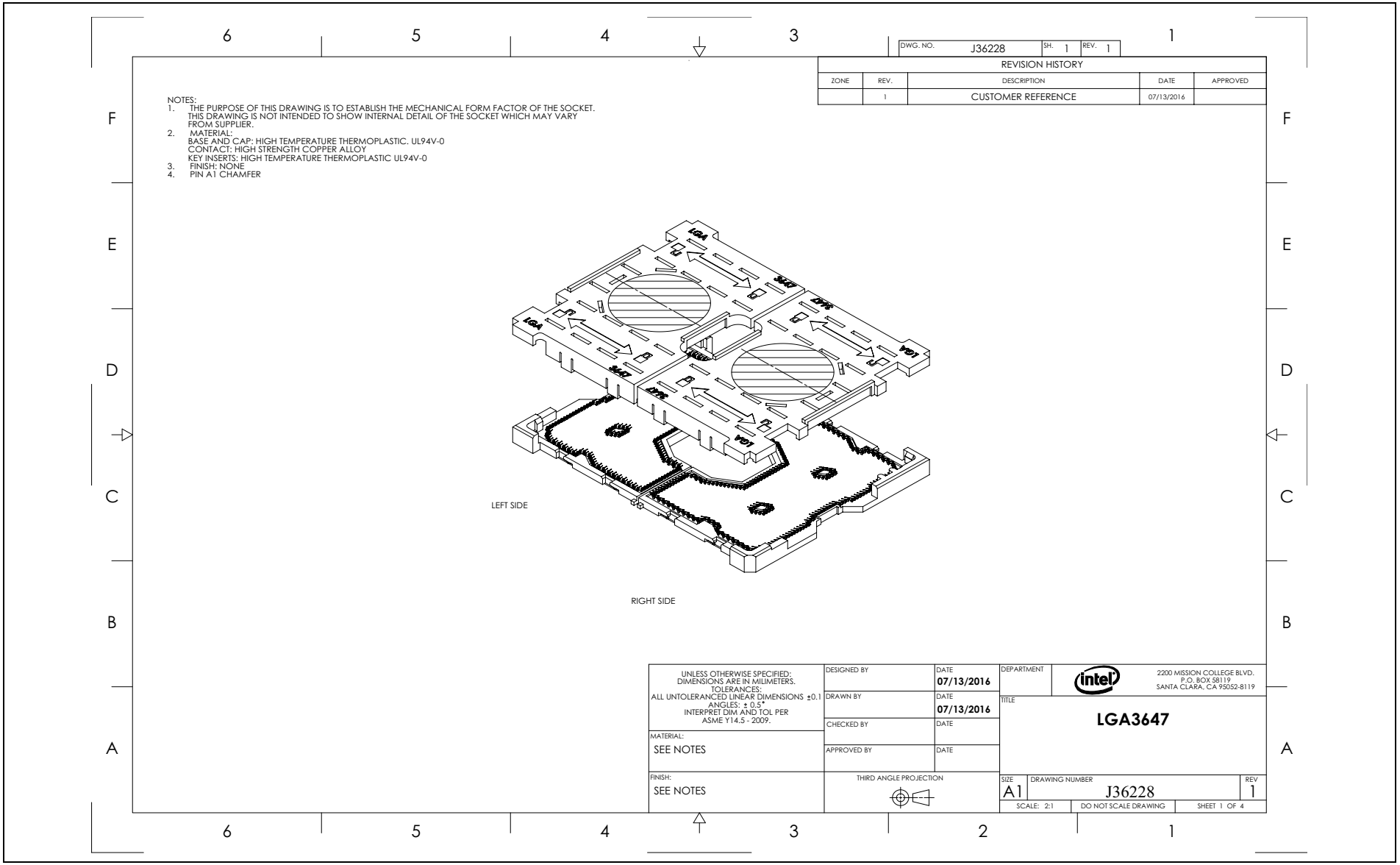
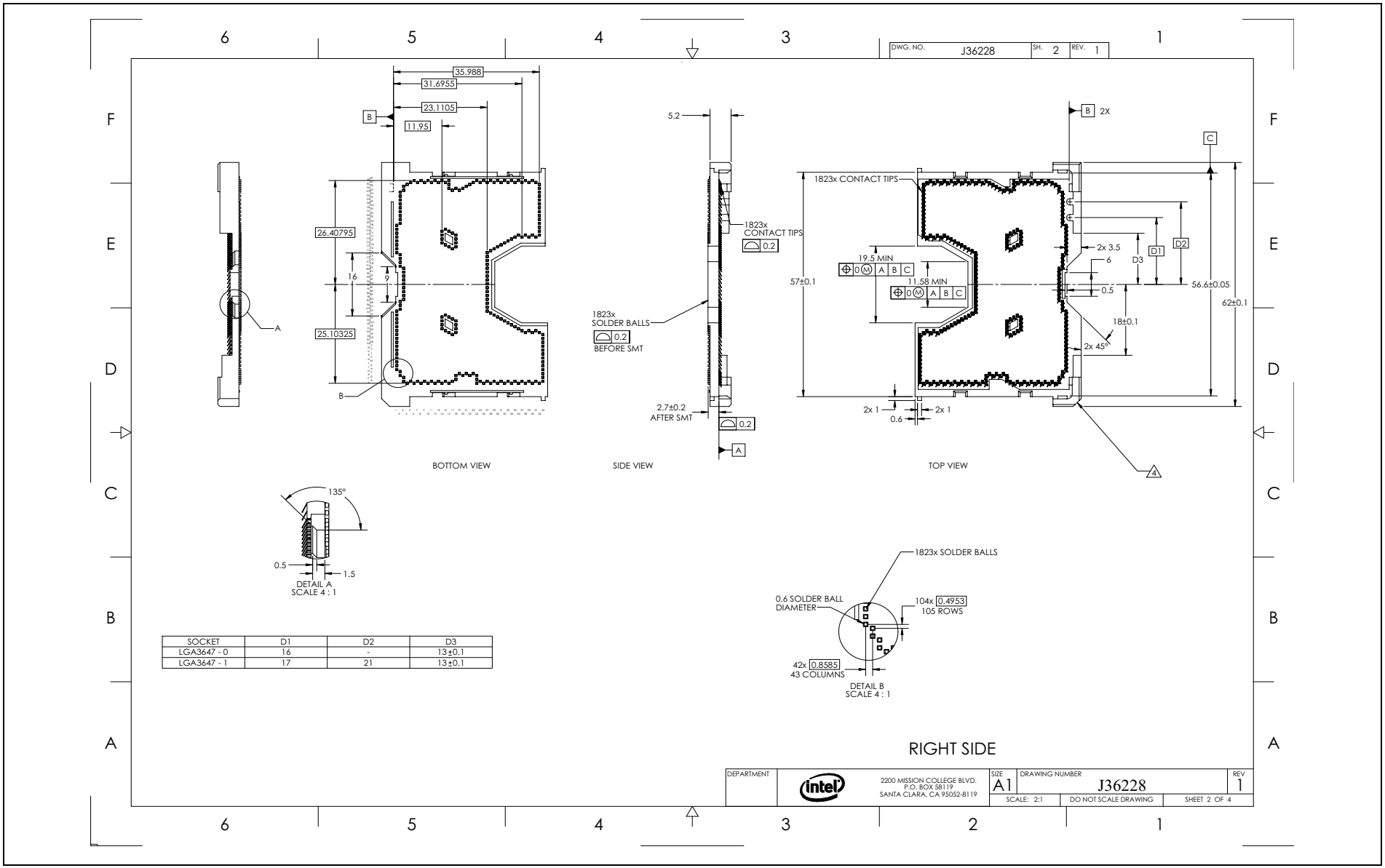
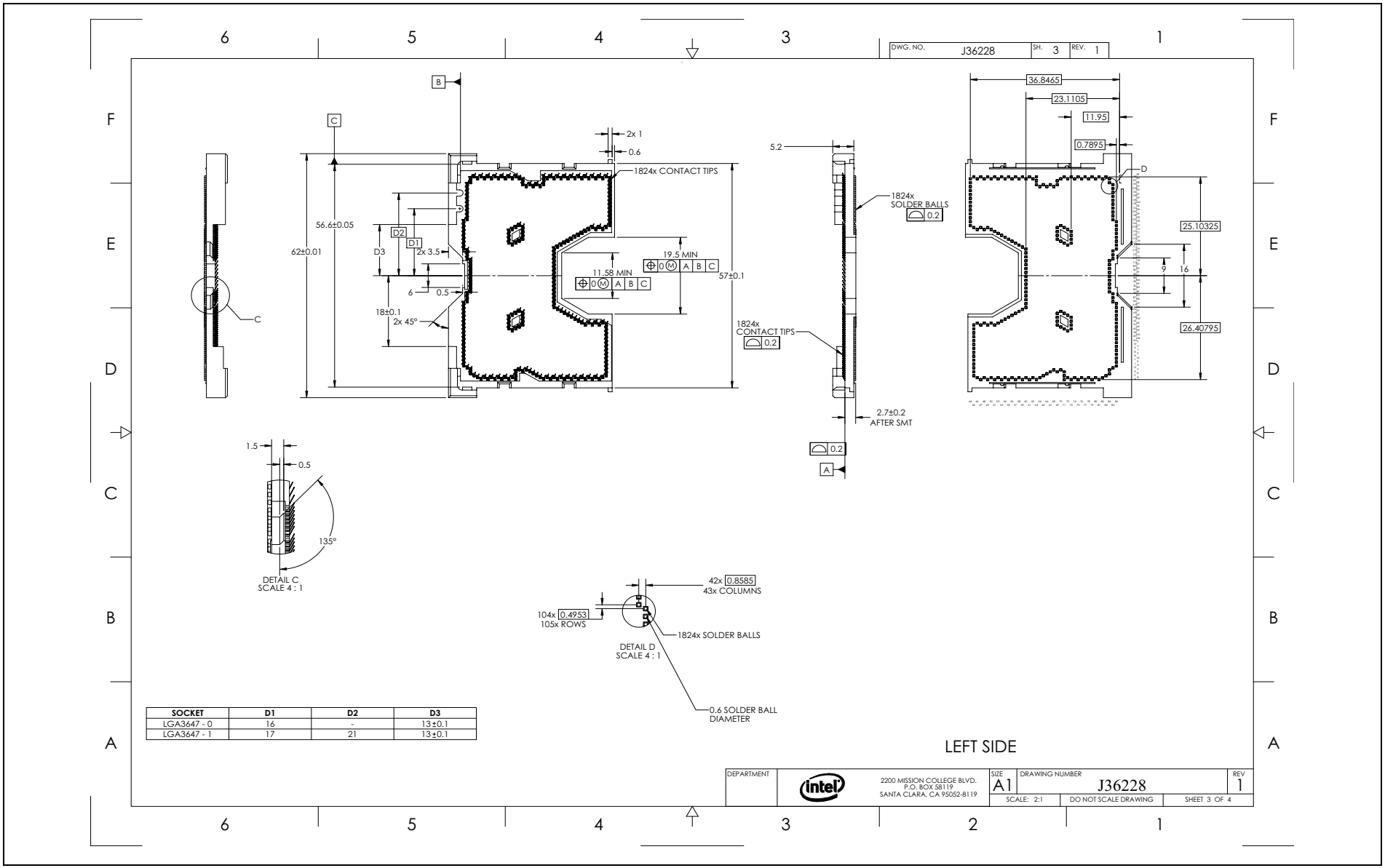


Figure C-1. Socket Mechanical Drawing (Sheet 2 of 4)



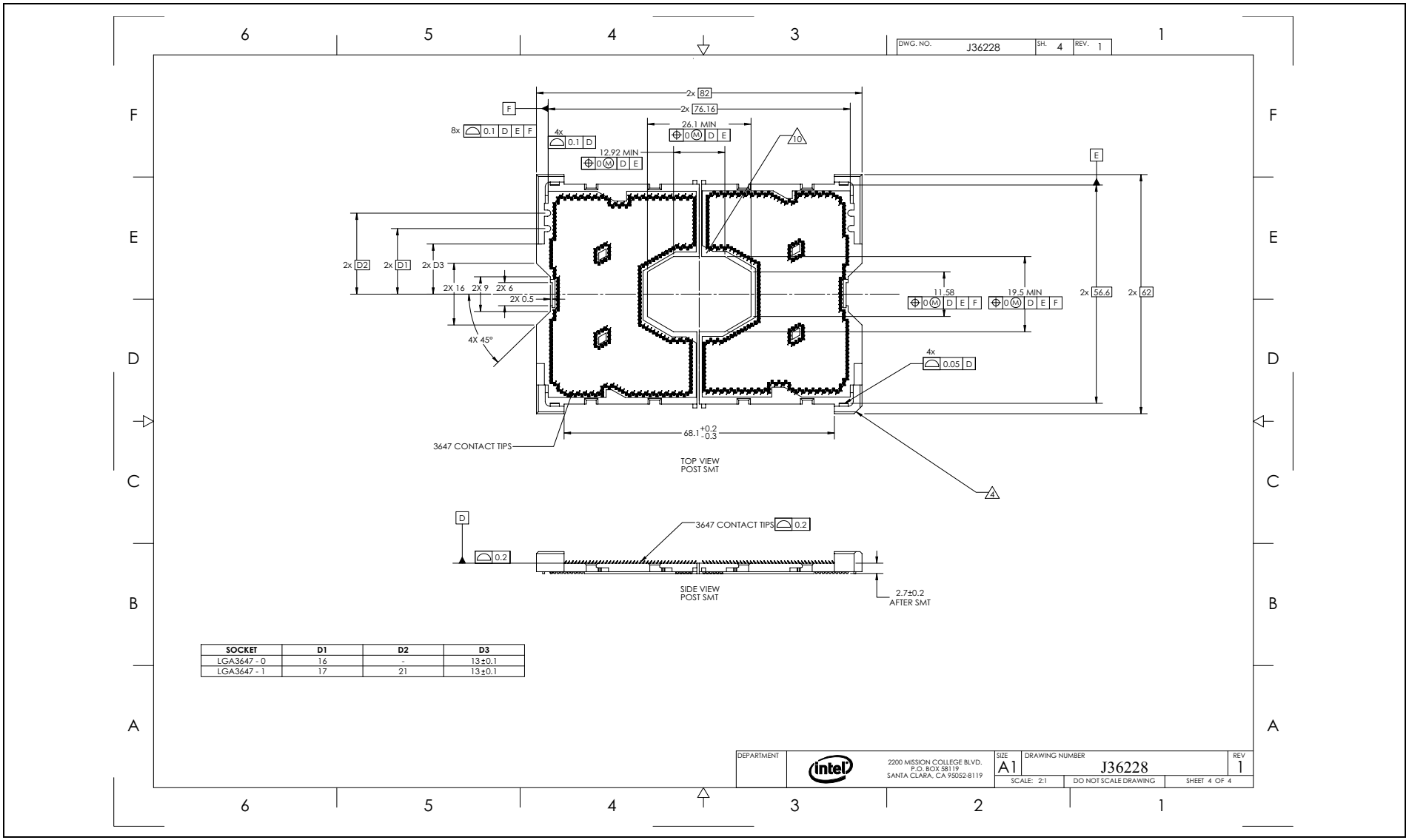
SOCKET	D1	D2	D3
LGA3647 - 0	16	-	13±0.1
LGA3647 - 1	17	21	13±0.1

Figure C-1. Socket Mechanical Drawing (Sheet 3 of 4)



SOCKET	D1	D2	D3
LGA3647 - 0	16	-	13±0.1
LGA3647 - 1	17	21	13±0.1

Figure C-1. Socket Mechanical Drawing (Sheet 4 of 4)



§

D Retention Assembly Mechanical Drawings

D.1 Processor Heatsink Loading Mechanism (PHLM) Drawings

Table D-1 lists the mechanical drawings that are used in the loading mechanism of the Second Generation Intel® Xeon® Scalable Processors based platform.

Table D-1. Second Generation Intel® Xeon® Scalable Processors Based Mechanical Drawing List

Description	Figure
Bolster Guide Post - Small	Figure D-1
Bolster Guide Post - Large	Figure D-2
Backplate Stud	Figure D-3
Spring Rivet	Figure D-4
Bolster Captive Nut	Figure D-5
Bolster Captive Nut Collar	Figure D-6
Narrow Backplate	Figure D-7
Narrow Backplate Insulator	Figure D-8
Narrow-Fabric Bolster Plate	Figure D-9
Narrow Bolster Plate	Figure D-10
Narrow Bolster Insulator	Figure D-11
Narrow CPU Carrier	Figure D-12
Narrow Backplate Assembly	Figure D-13
Narrow Dust Cover	Figure D-14
Narrow Spring Assembly	Figure D-15
Narrow Spring	Figure D-16
Narrow - Fabric Bolster Plate Assembly	Figure D-17
Narrow Bolster Plate Assembly	Figure D-18
Bolster Corner Standoff	Figure D-19
Narrow Spring Stud	Figure D-20
Backplate Stud: Long	Figure D-21
Narrow Backplate Long Stud Assembly	Figure D-22

D.2 PHLM Narrow (NRW) Drawings

Table D-2 lists the mechanical drawings included in the NRW processor heatsink loading mechanism configuration.

Table D-2. NRW Mechanical Drawing List

Description	Figure
Narrow Bolster Plate Assembly	Figure D-18
• Bolster Guide Post - Small	Figure D-1
• Bolster Guide Post - Large	Figure D-2
• Spring Rivet	Figure D-4
• Bolster Captive Nut	Figure D-5
• Bolster Captive Nut Collar	Figure D-6
• Narrow Bolster Plate	Figure D-10
• Narrow Bolster Insulator	Figure D-11
• Narrow Spring Assembly	Figure D-15
— Narrow Spring Stud	Figure D-20
— Narrow Spring	Figure D-16
• Bolster Corner Standoff	Figure D-19
Narrow Backplate Assembly	Figure D-13
• Backplate Stud	Figure D-3
• Narrow Backplate	Figure D-7
• Narrow Backplate Insulator	Figure D-8
Narrow Backplate Long Stud Assembly	Figure D-22
• Backplate Stud: Long	Figure D-21
• Narrow Backplate	Figure D-7
• Narrow Backplate Insulator	Figure D-8
Narrow Dust Cover	Figure D-14
Narrow CPU Carrier	Figure D-12

Figure D-1. Bolster Guide Post - Small

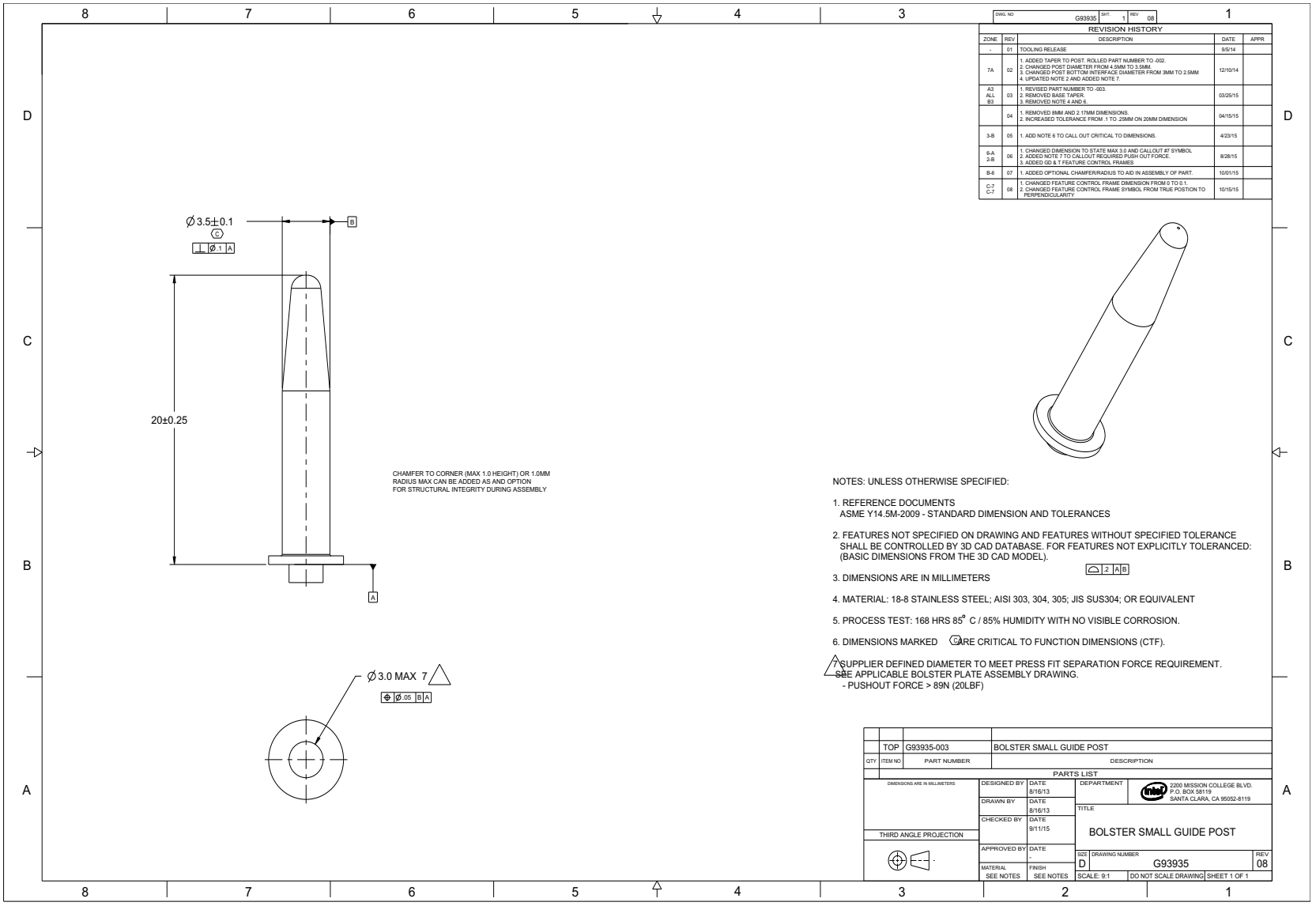


Figure D-2. Bolster Guide Post - Large

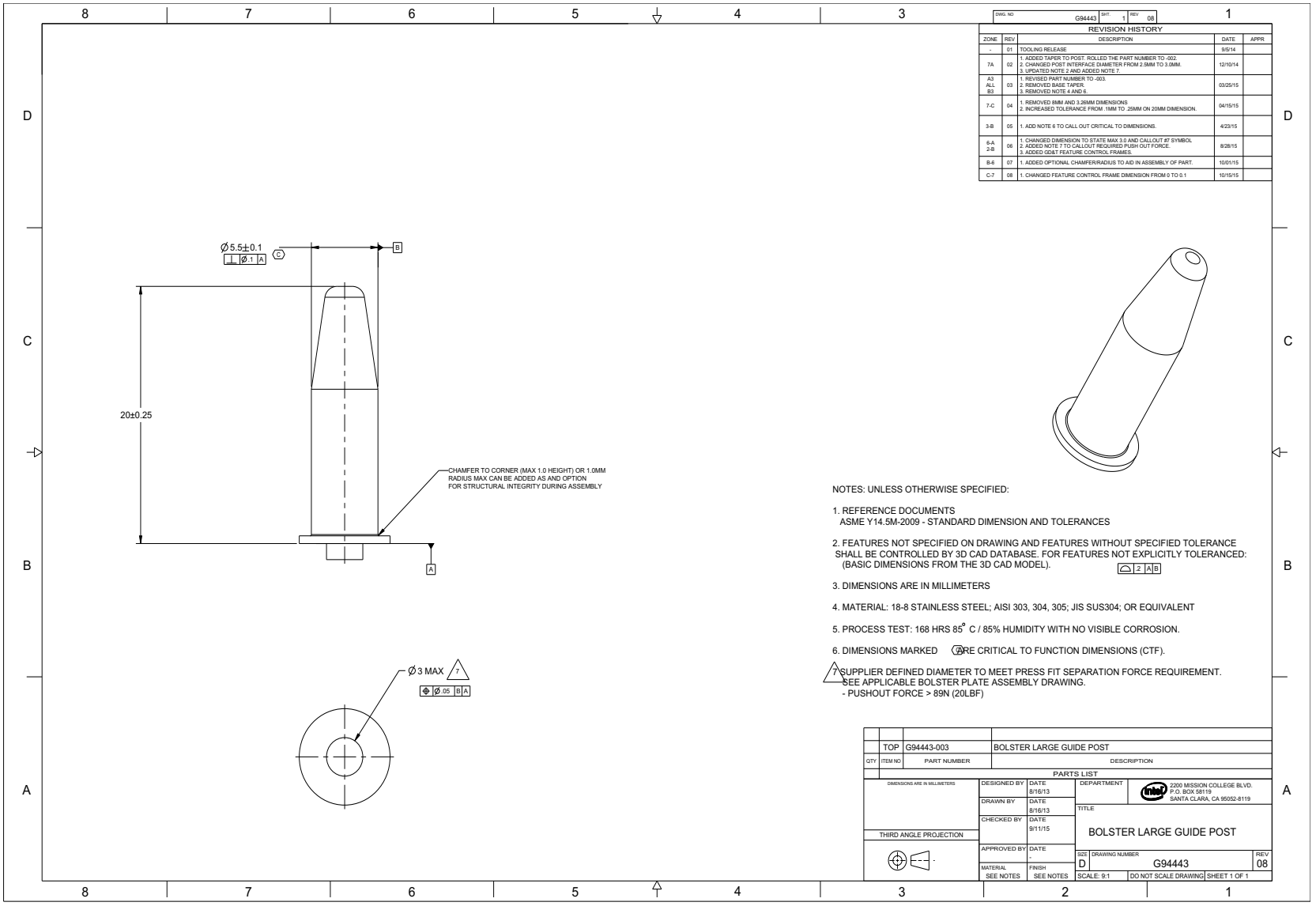


Figure D-3. Backplate Stud

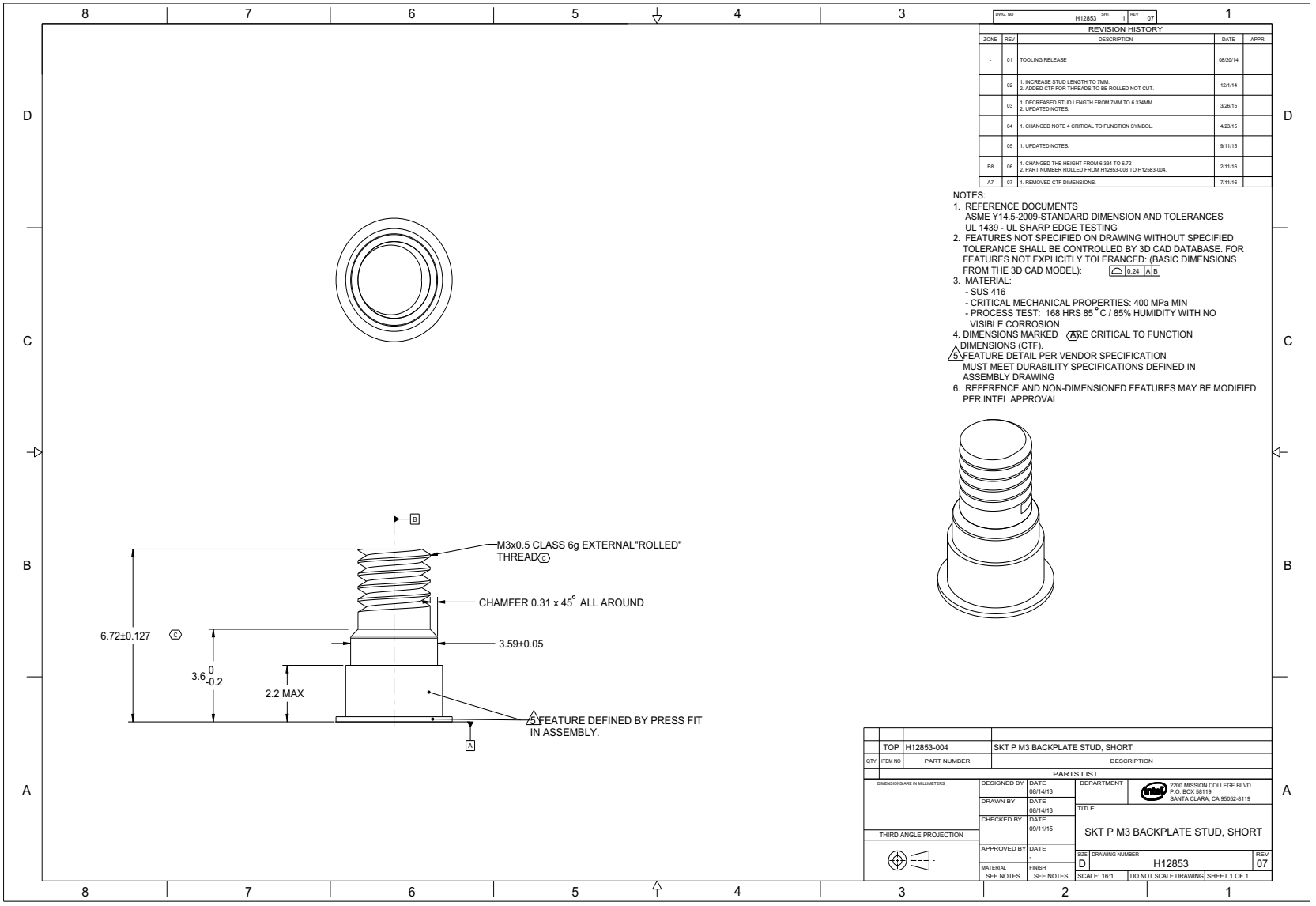


Figure D-4. Spring Rivet

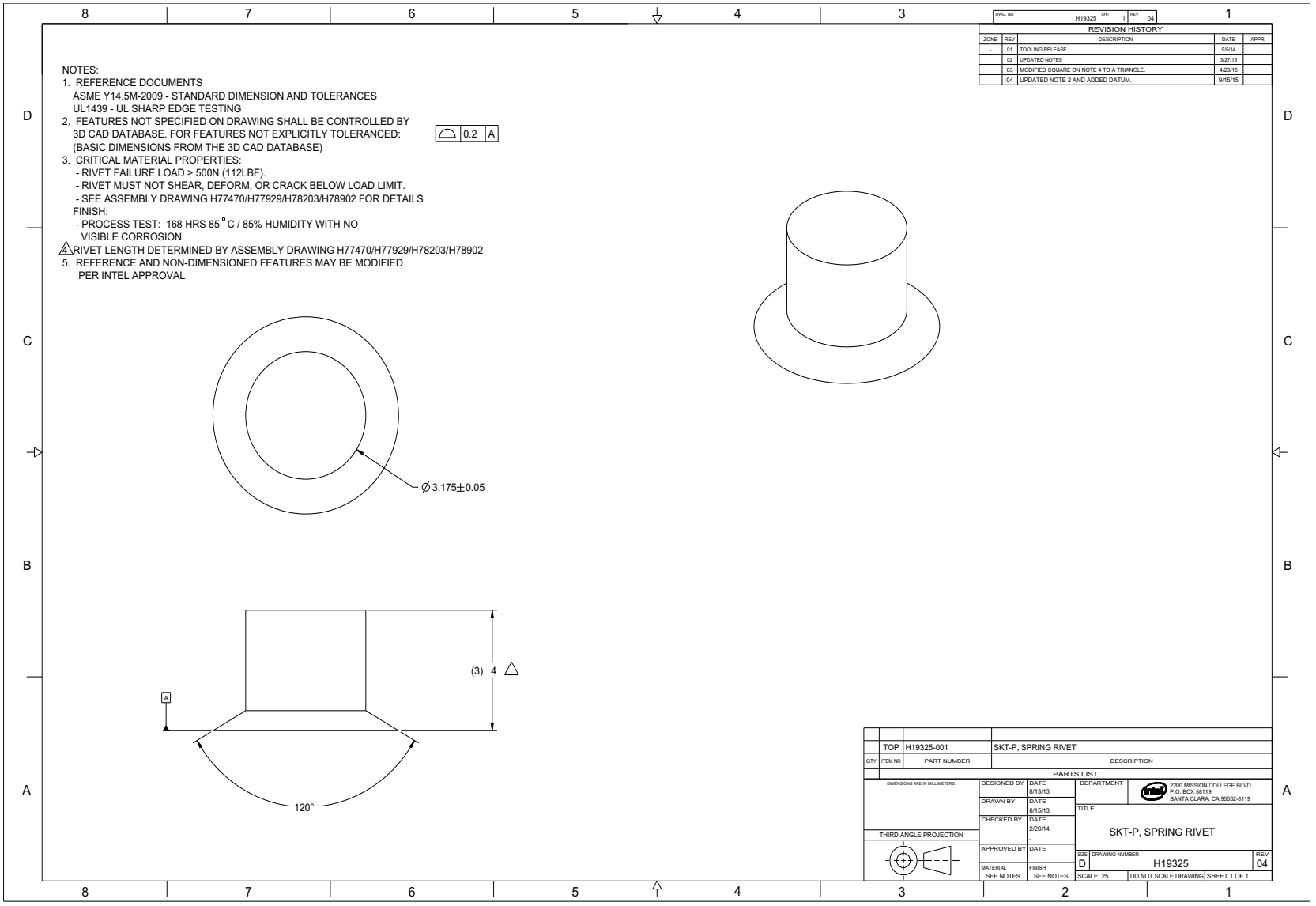


Figure D-5. Bolster Captive Nut

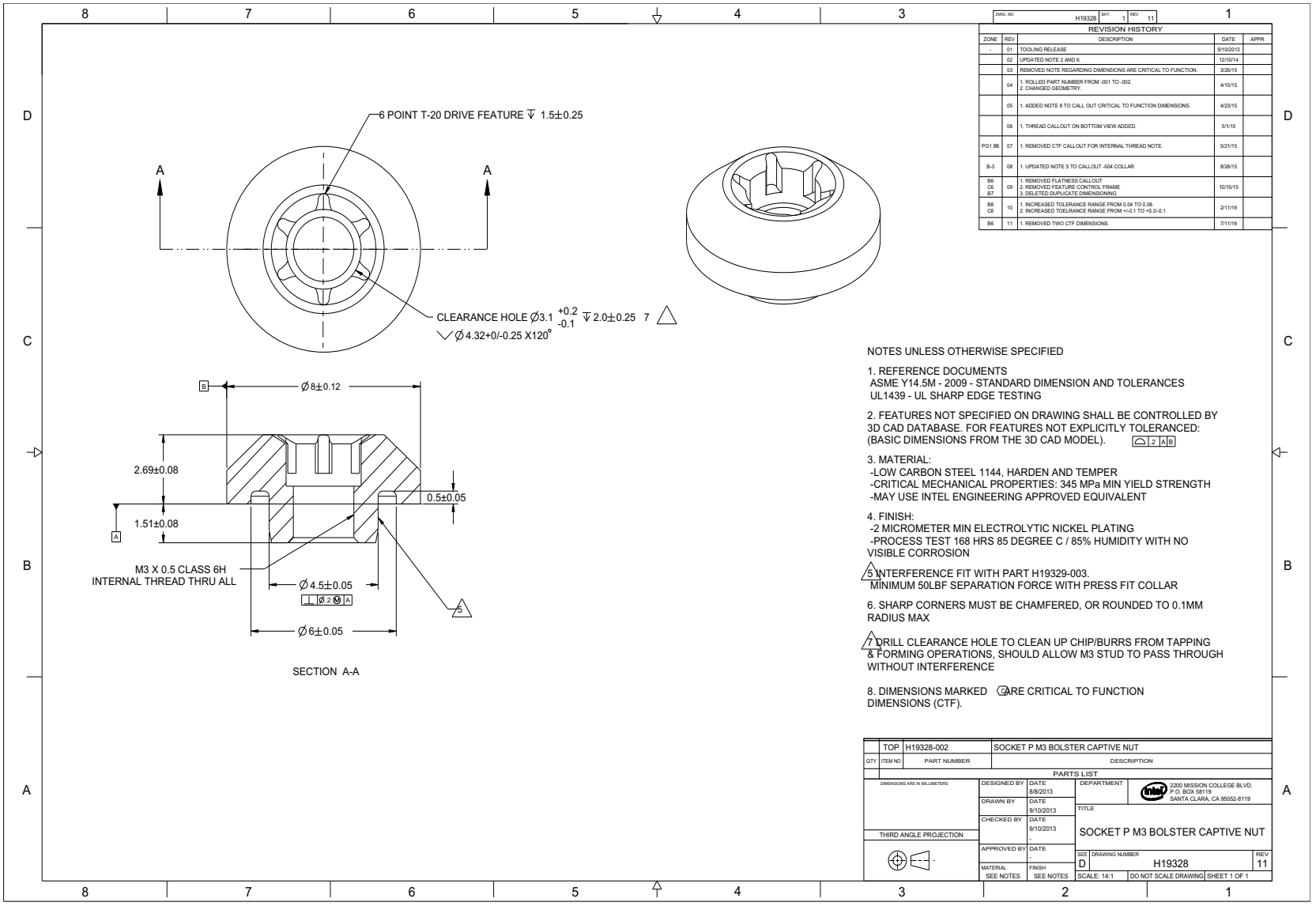


Figure D-6. Bolster Captive Nut Collar

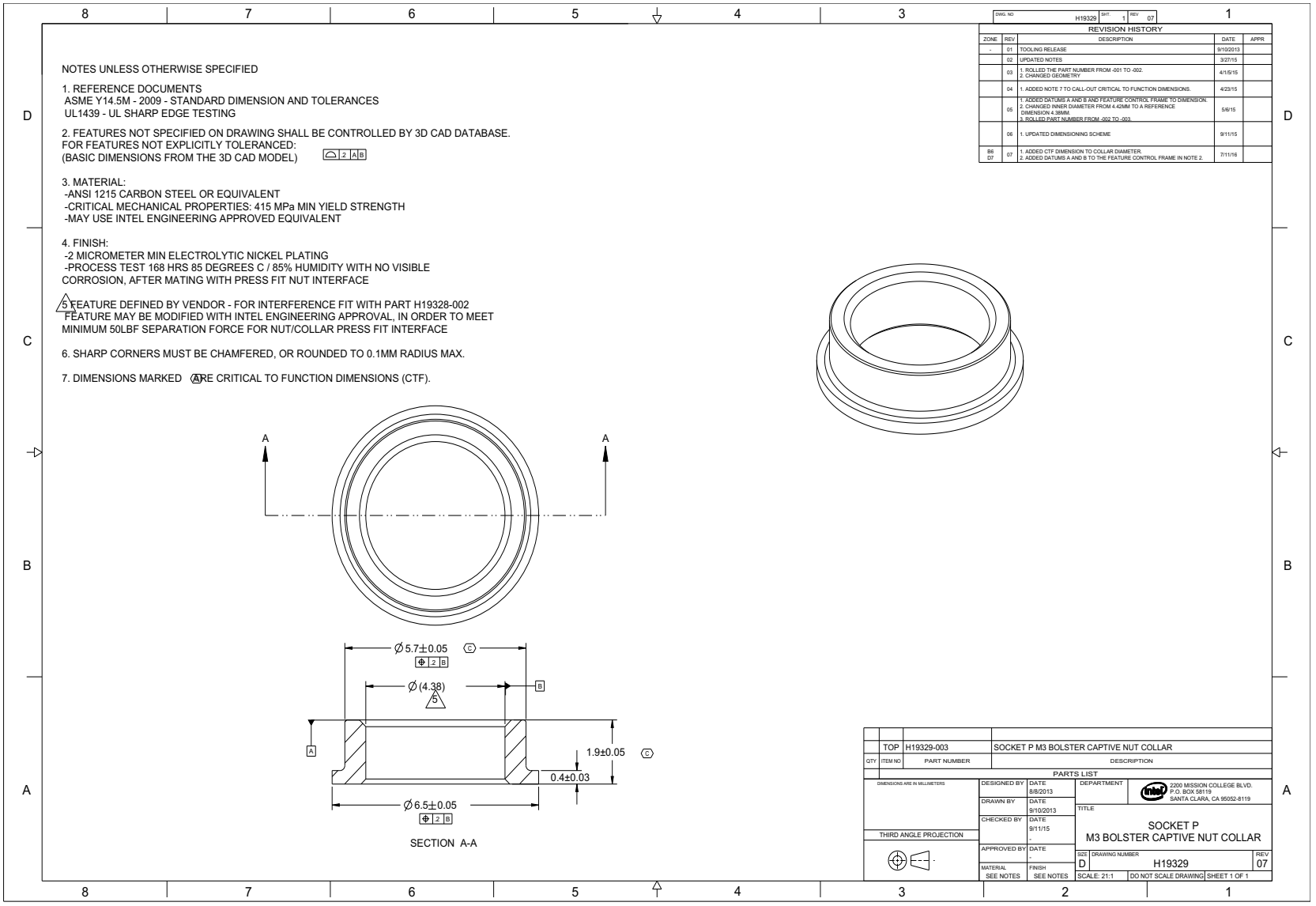


Figure D-7. Narrow Backplate

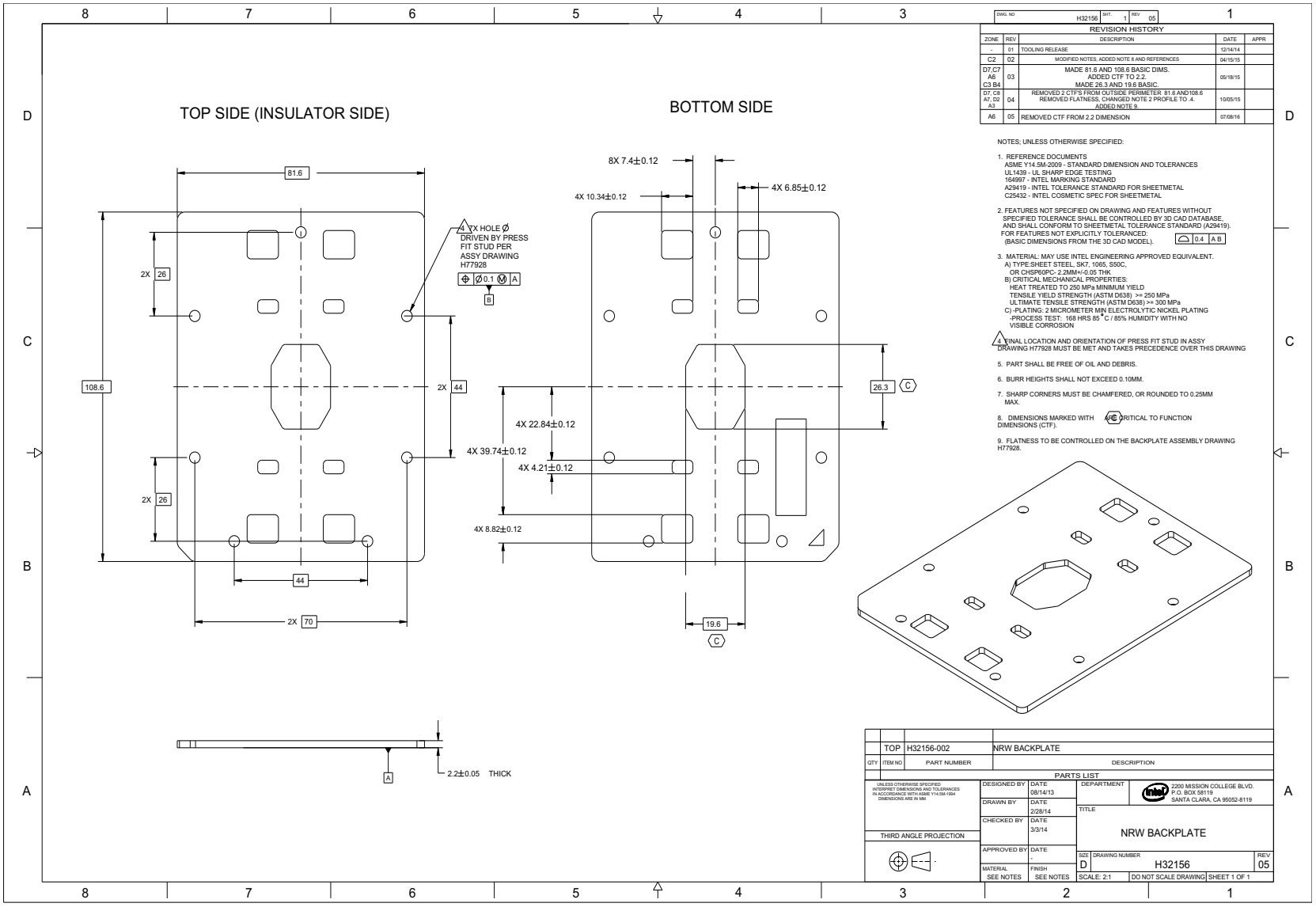


Figure D-8. Narrow Backplate Insulator

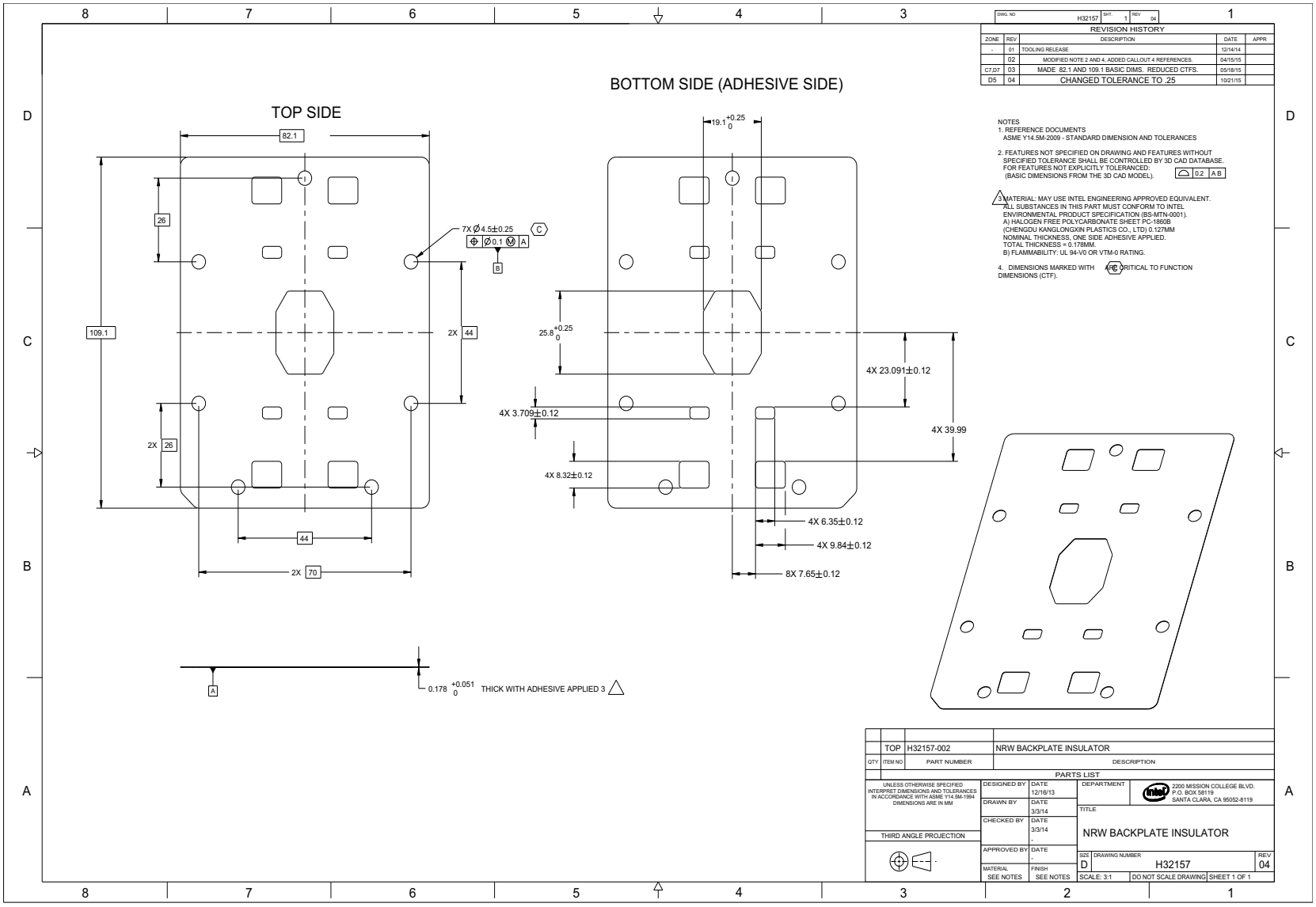


Figure D-9. Narrow-Fabric Bolster Plate (Sheet 1 of 3)

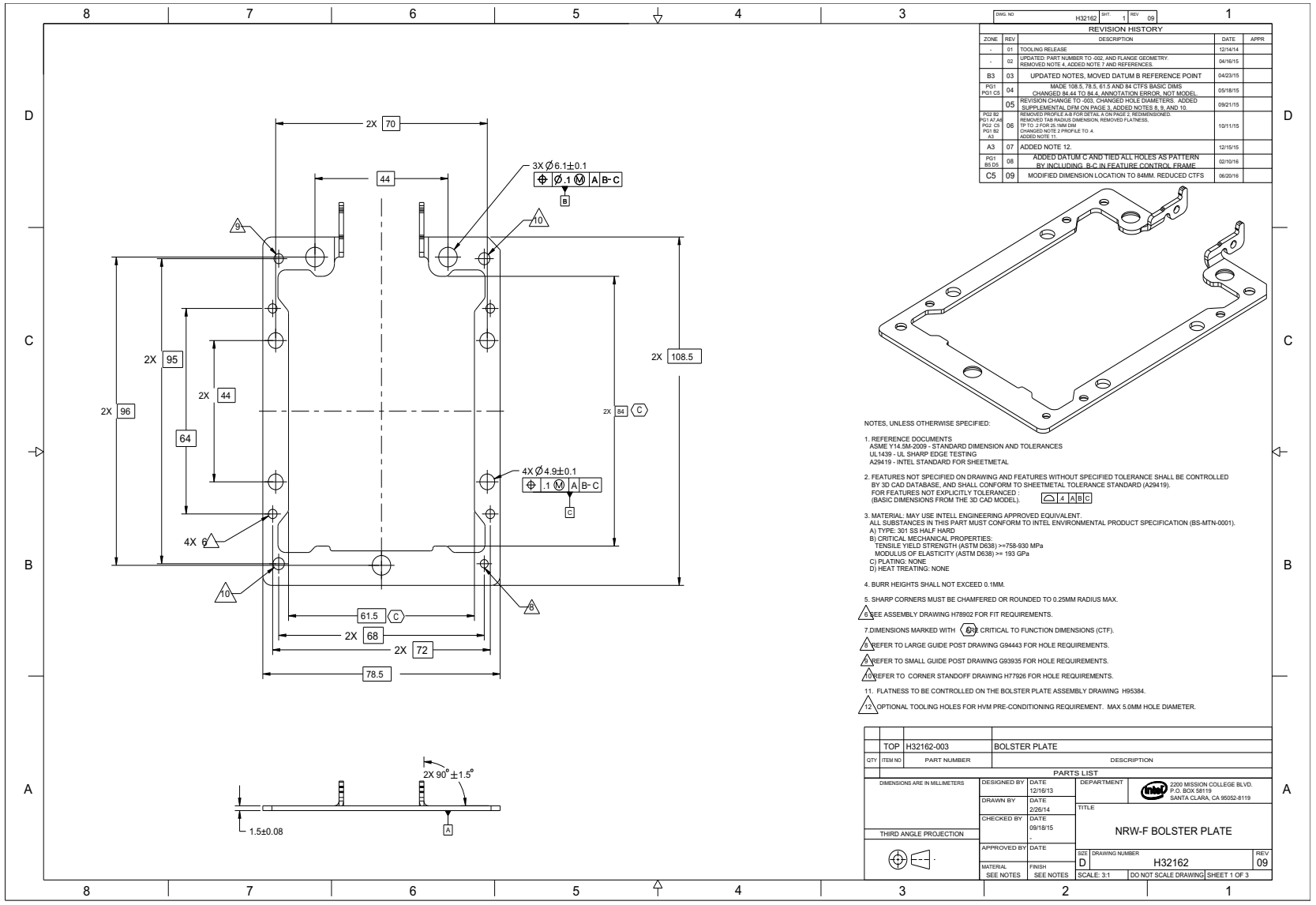


Figure D-9. Narrow-Fabric Bolster Plate (Sheet 2 of 3)

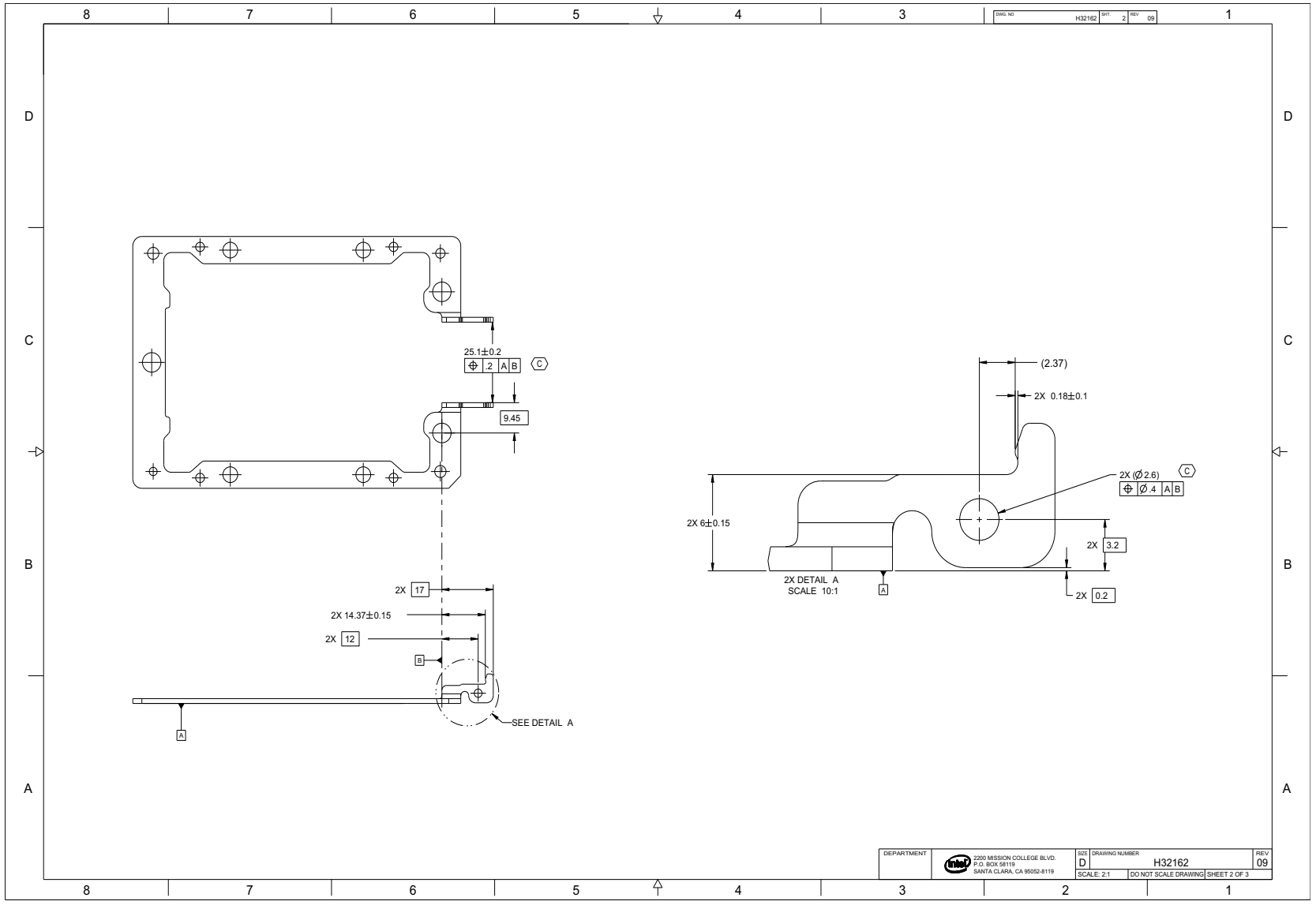


Figure D-9. Narrow-Fabric Bolster Plate (Sheet 3 of 3)

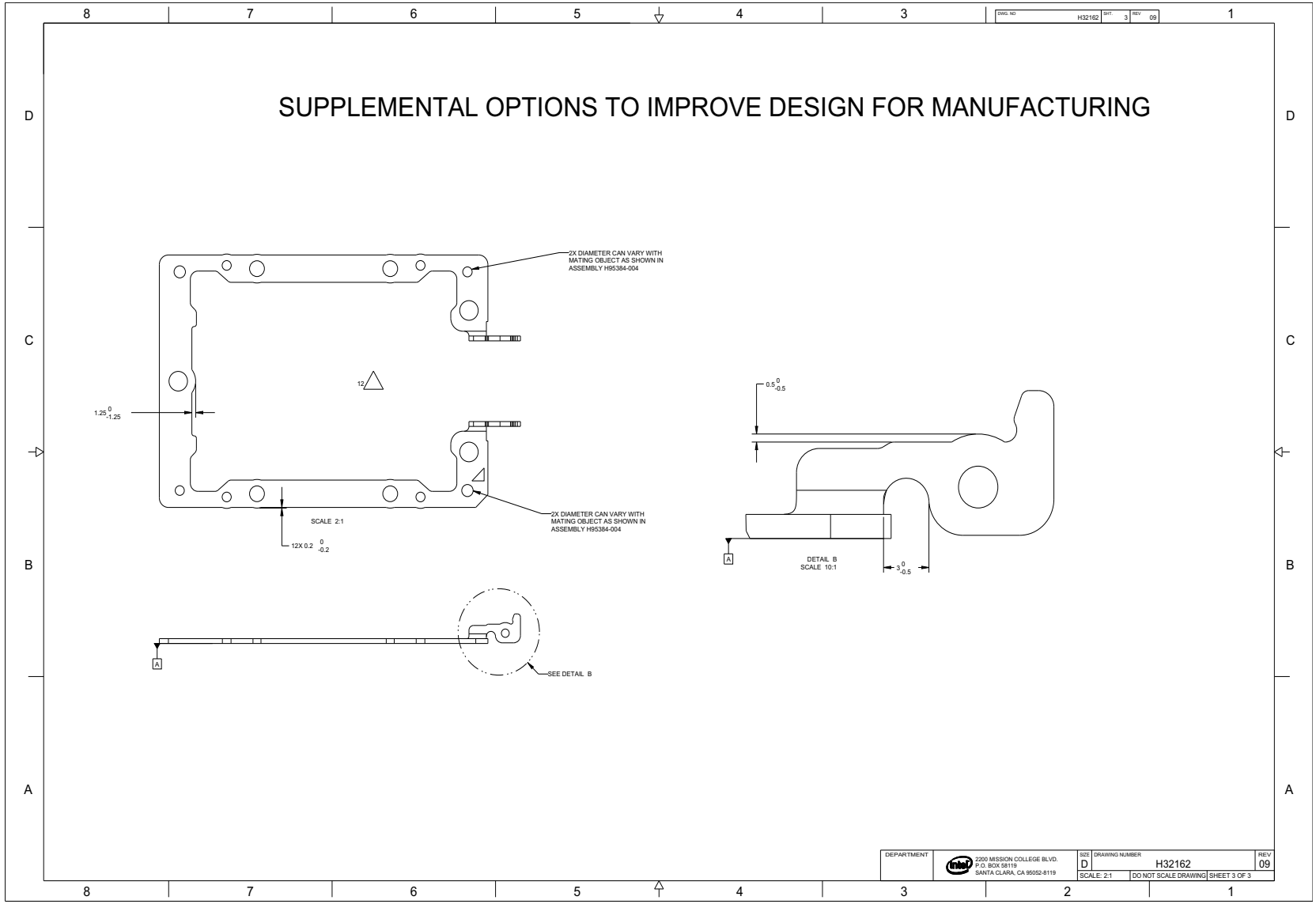


Figure D-10. Narrow Bolster Plate (Sheet 1 of 3)

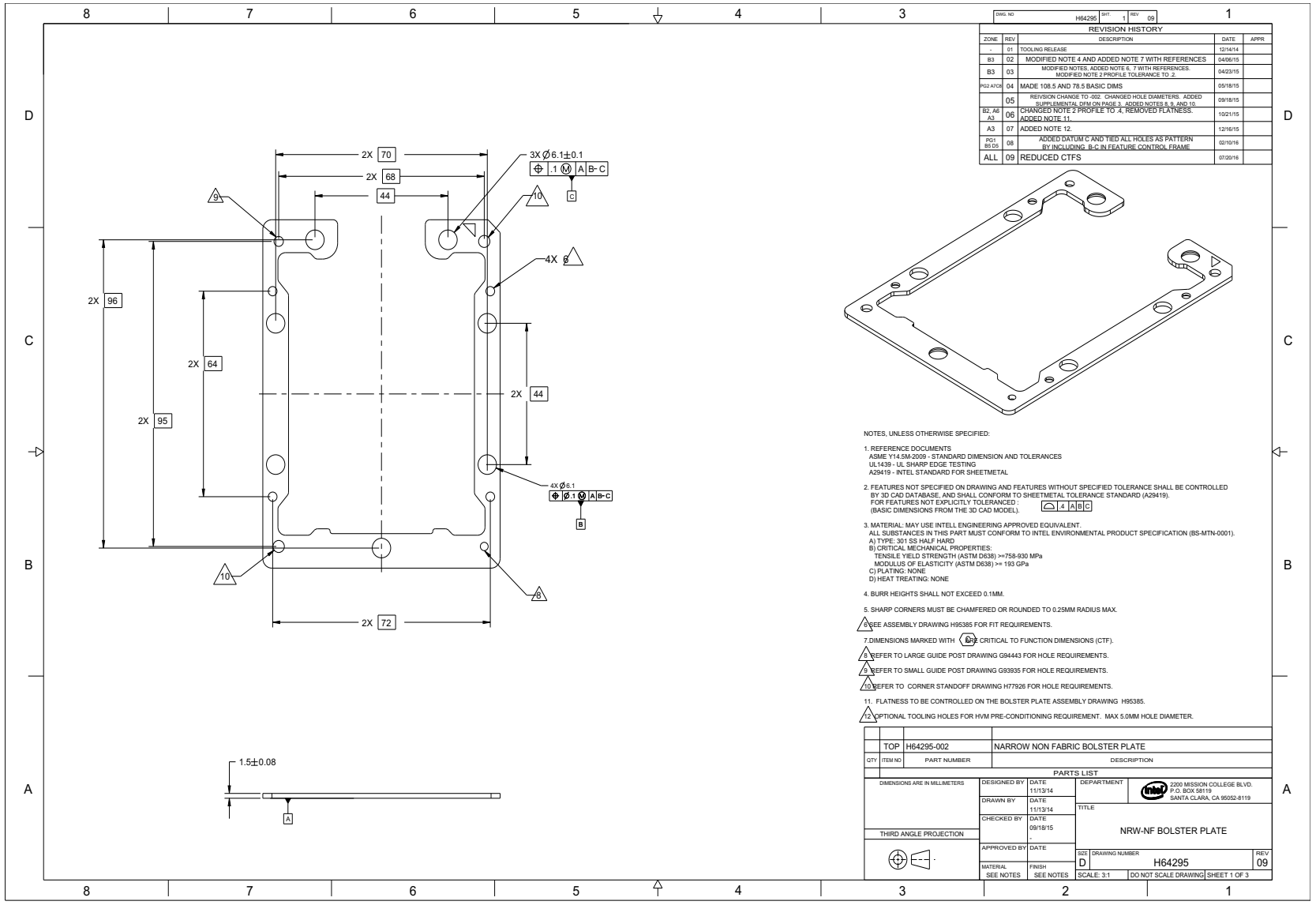


Figure D-10. Narrow Bolster Plate (Sheet 2 of 3)

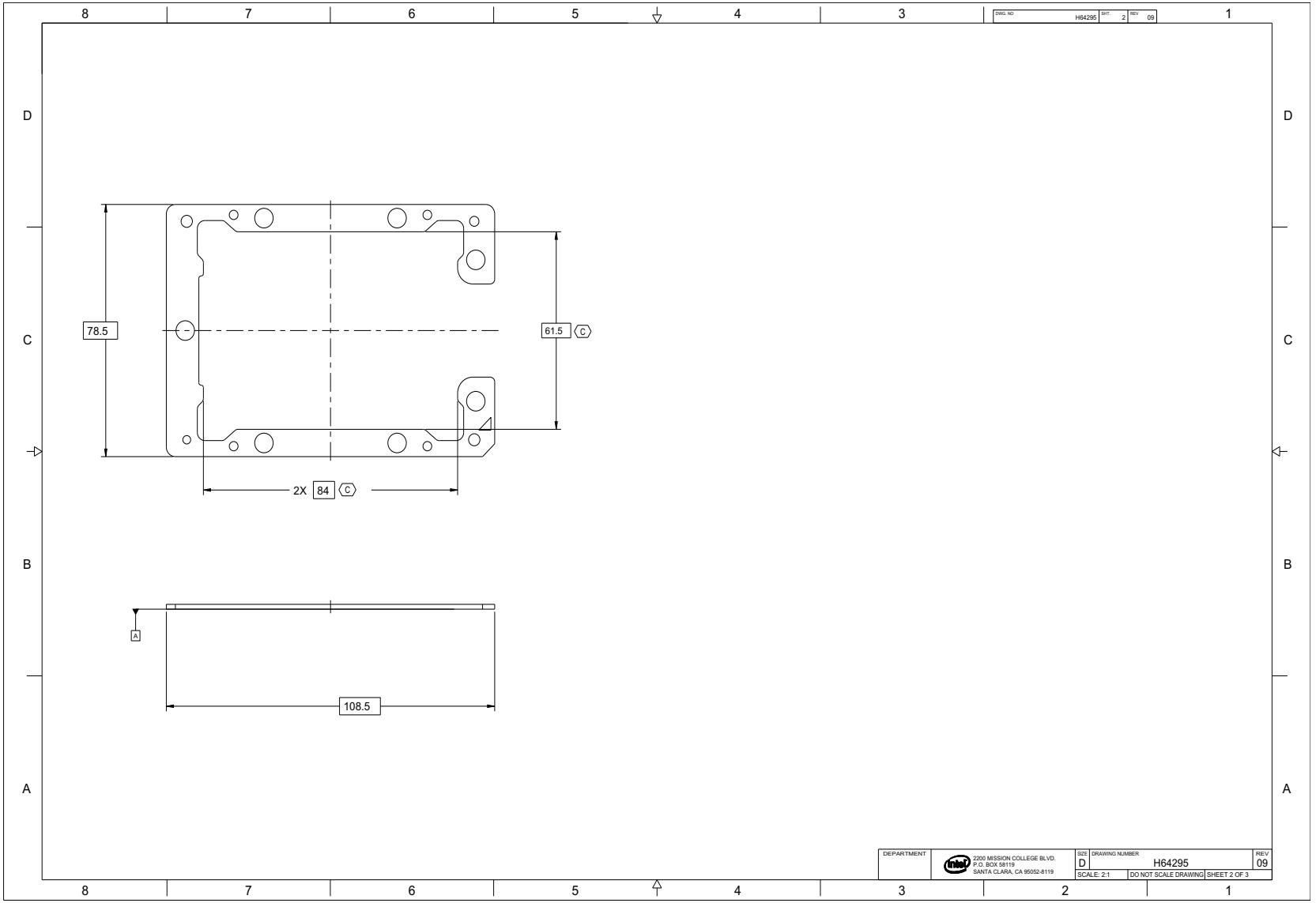


Figure D-10. Narrow Bolster Plate (Sheet 3 of 3)

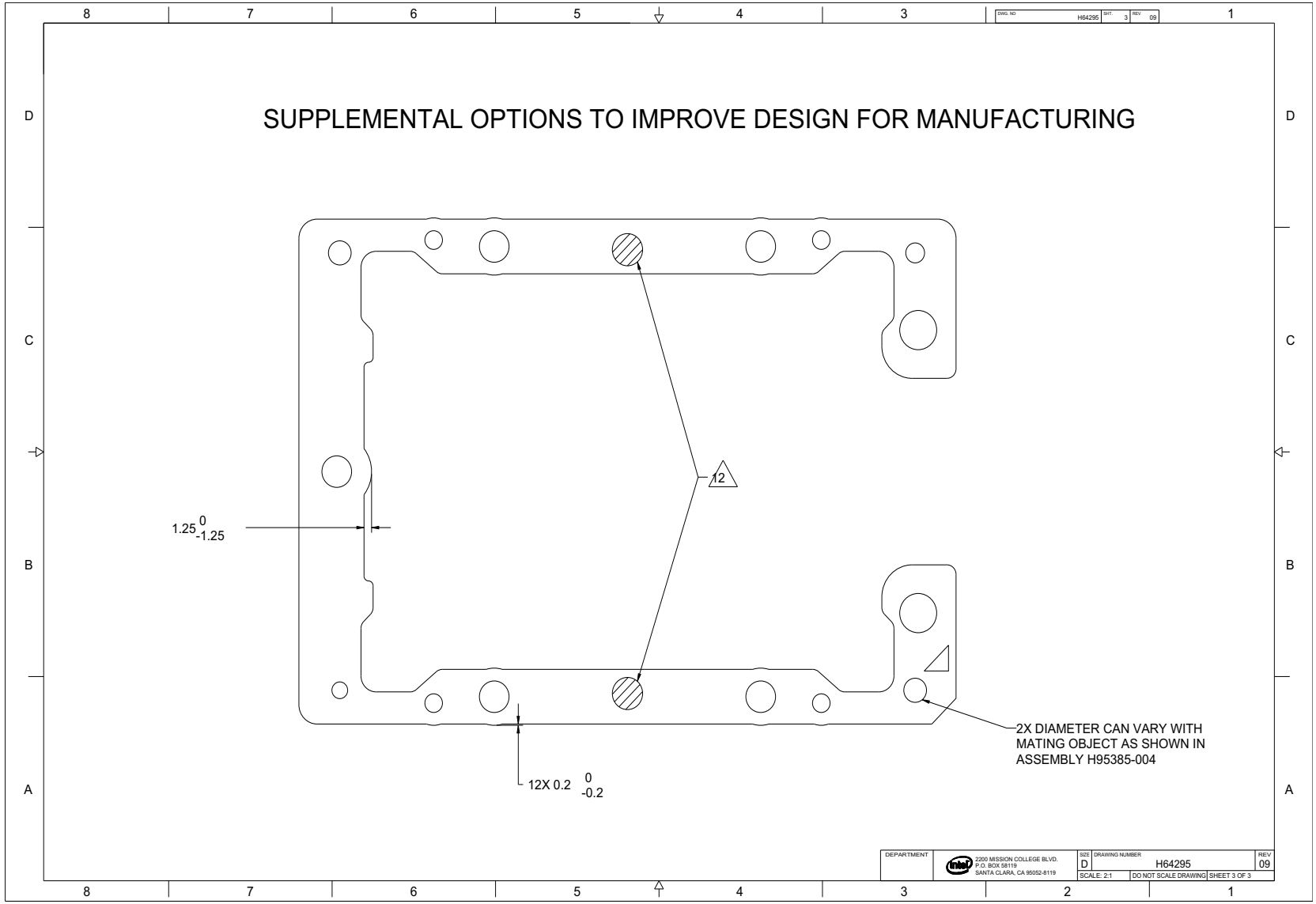


Figure D-11. Narrow Bolster Insulator

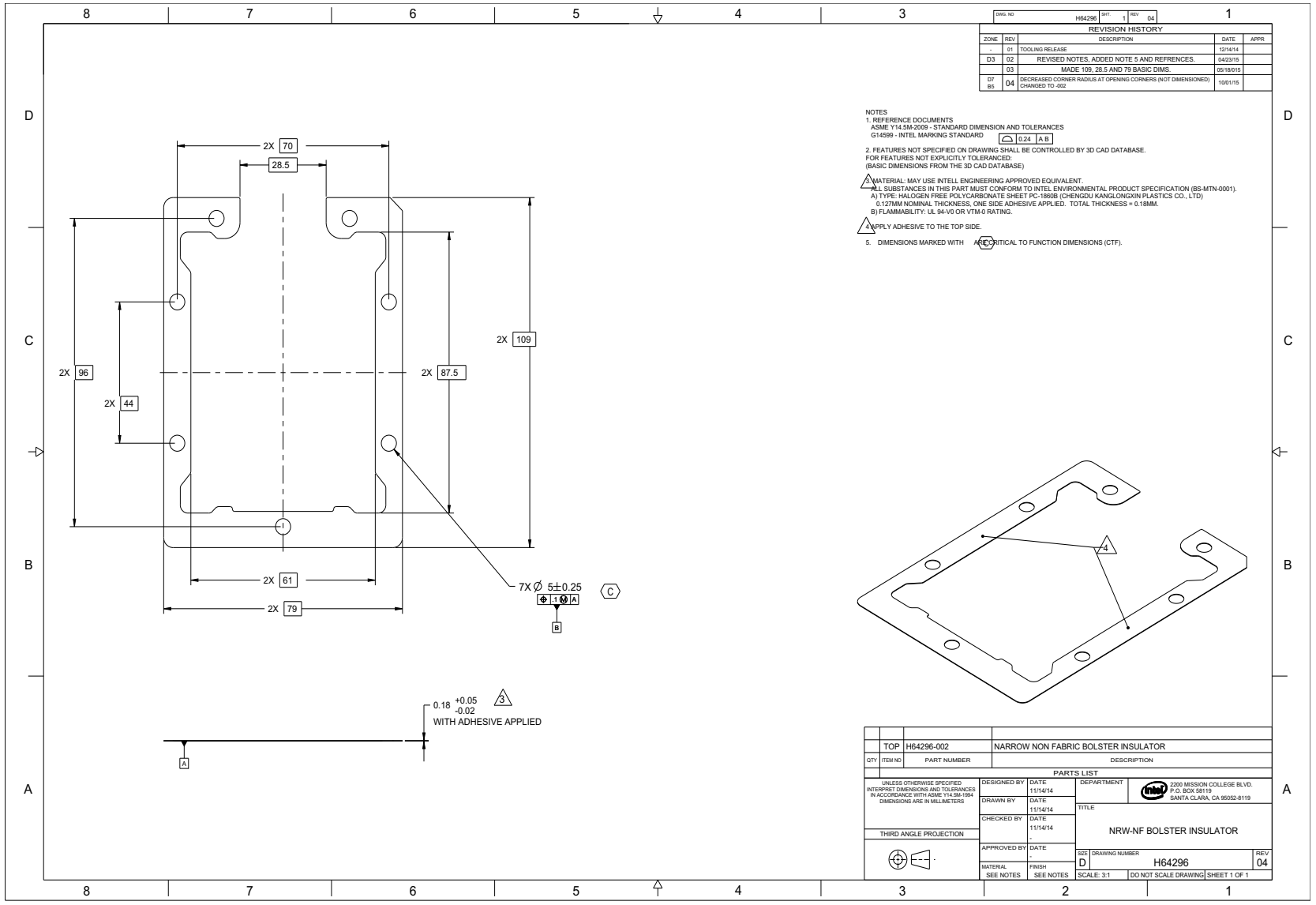


Figure D-12. Narrow CPU Carrier (Sheet 1 of 2)

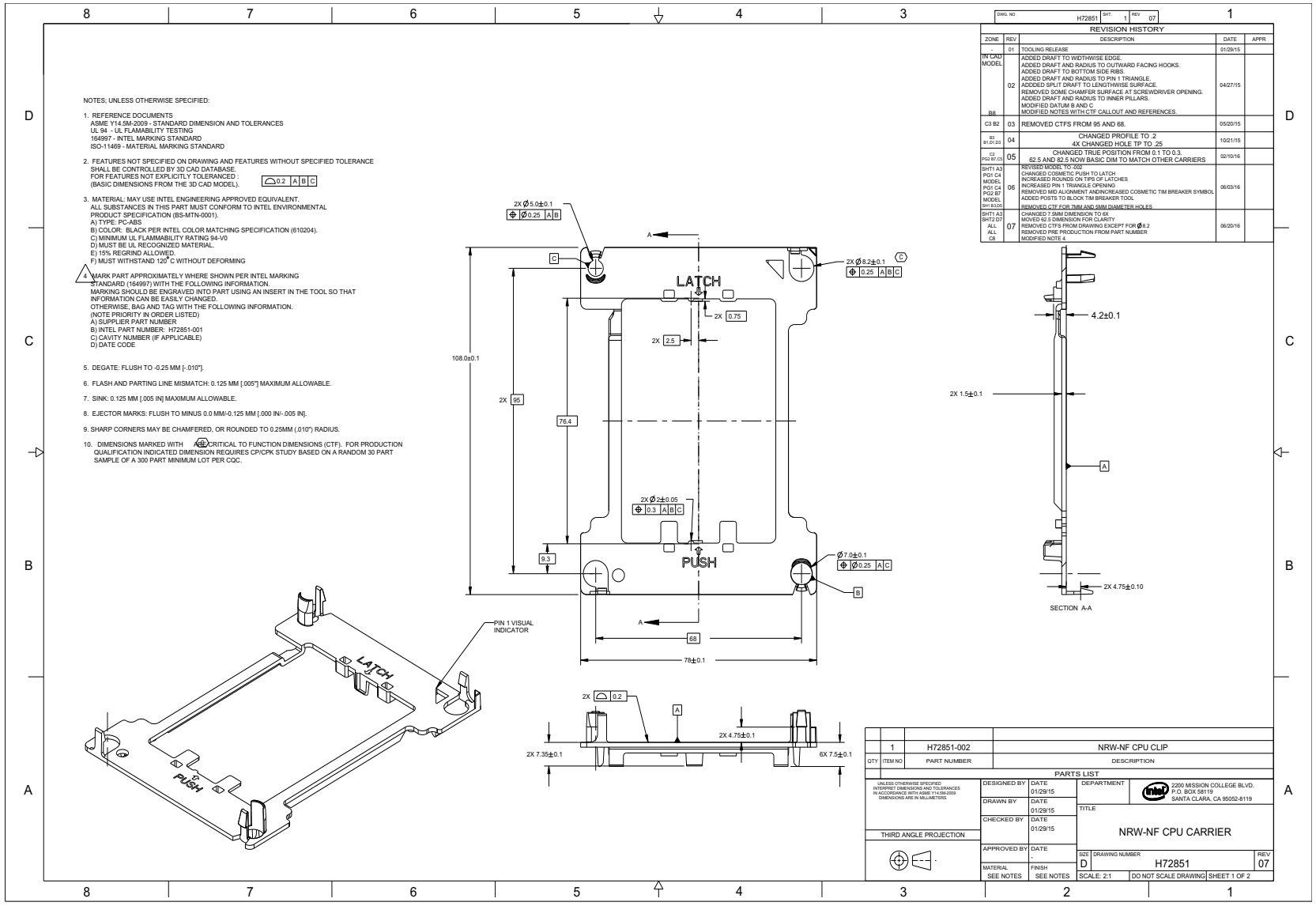


Figure D-12. Narrow CPU Carrier (Sheet 2 of 2)

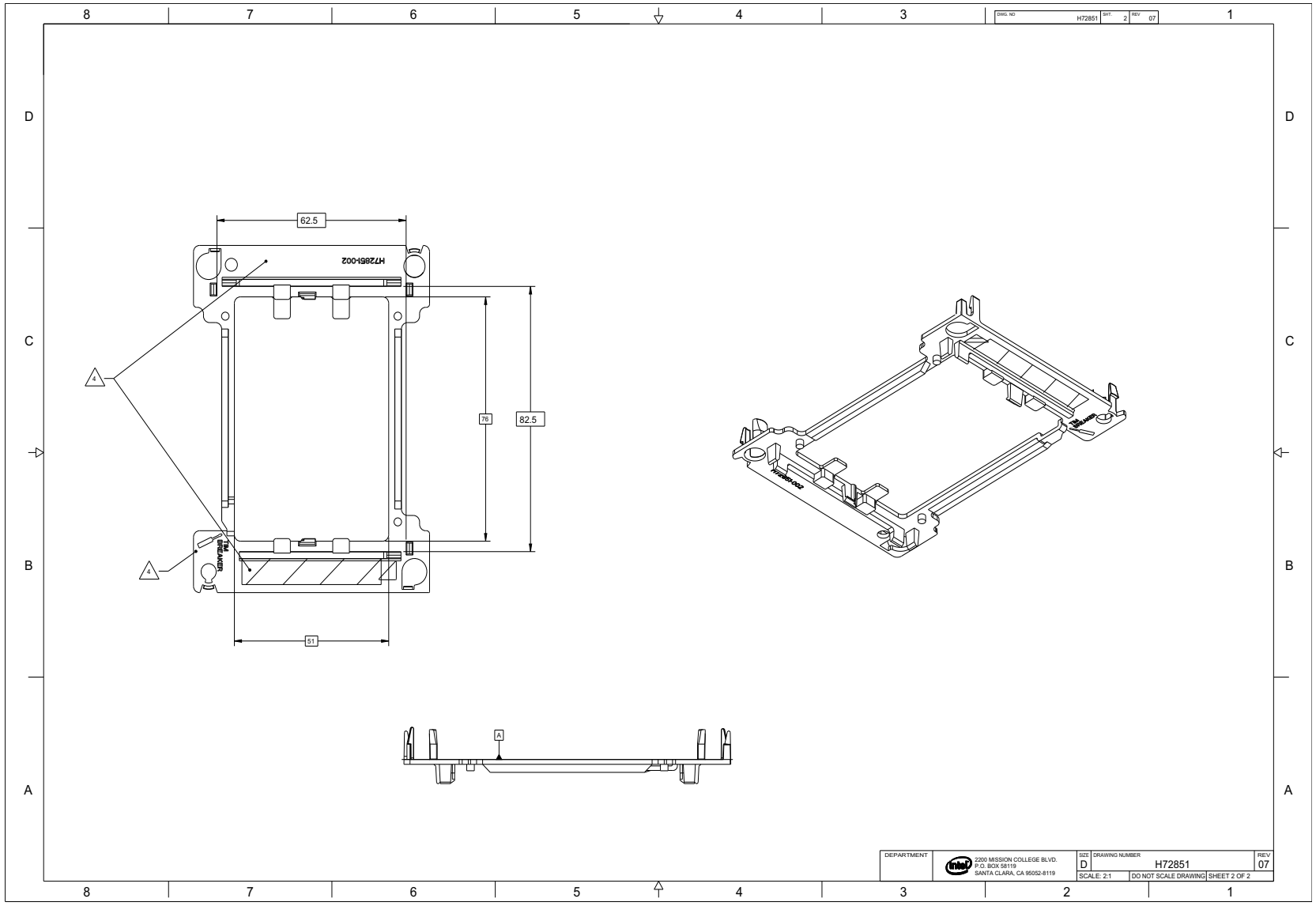


Figure D-13. Narrow Backplate Assembly (Sheet 1 of 2)

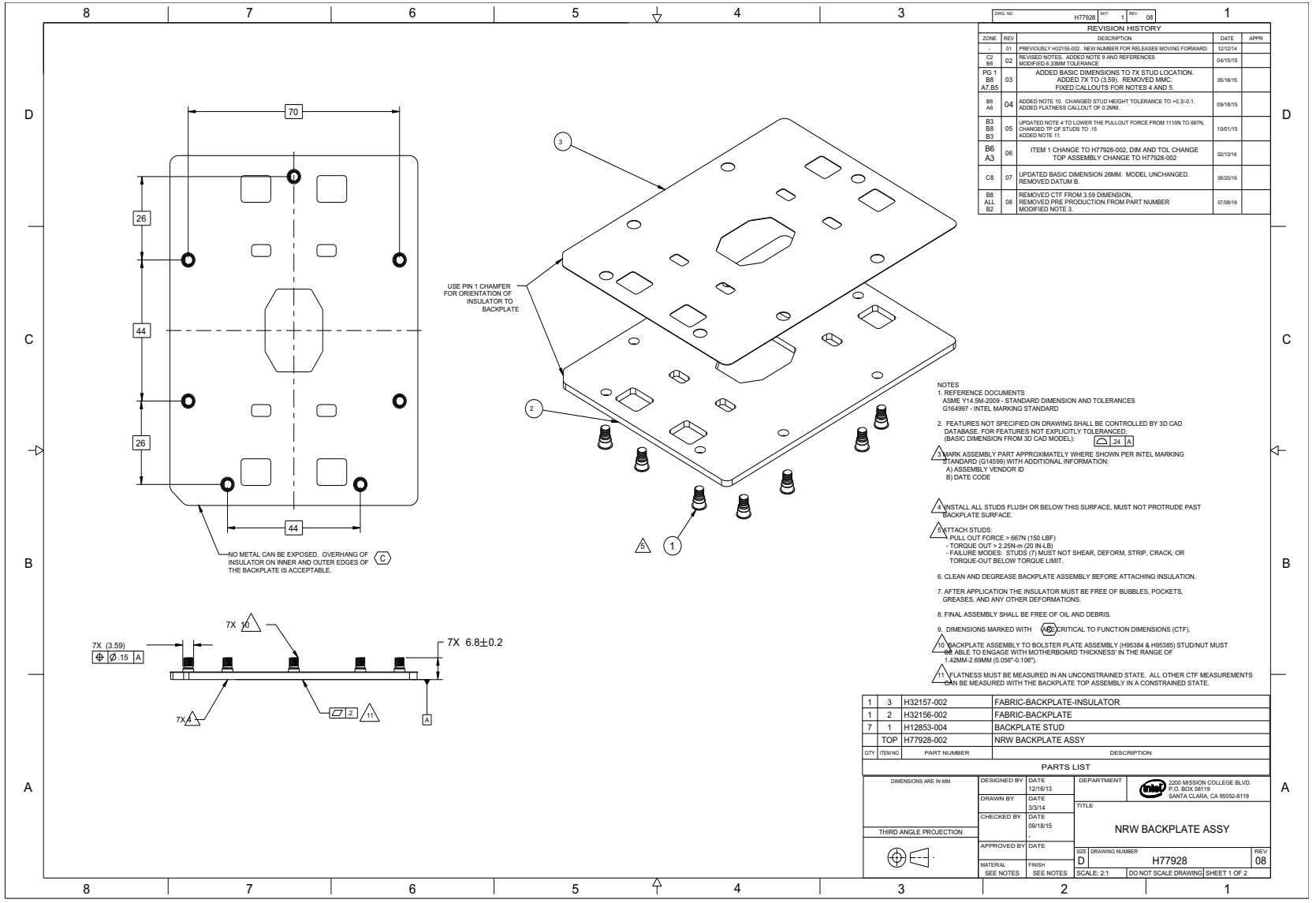


Figure D-13. Narrow Backplate Assembly (Sheet 2 of 2)

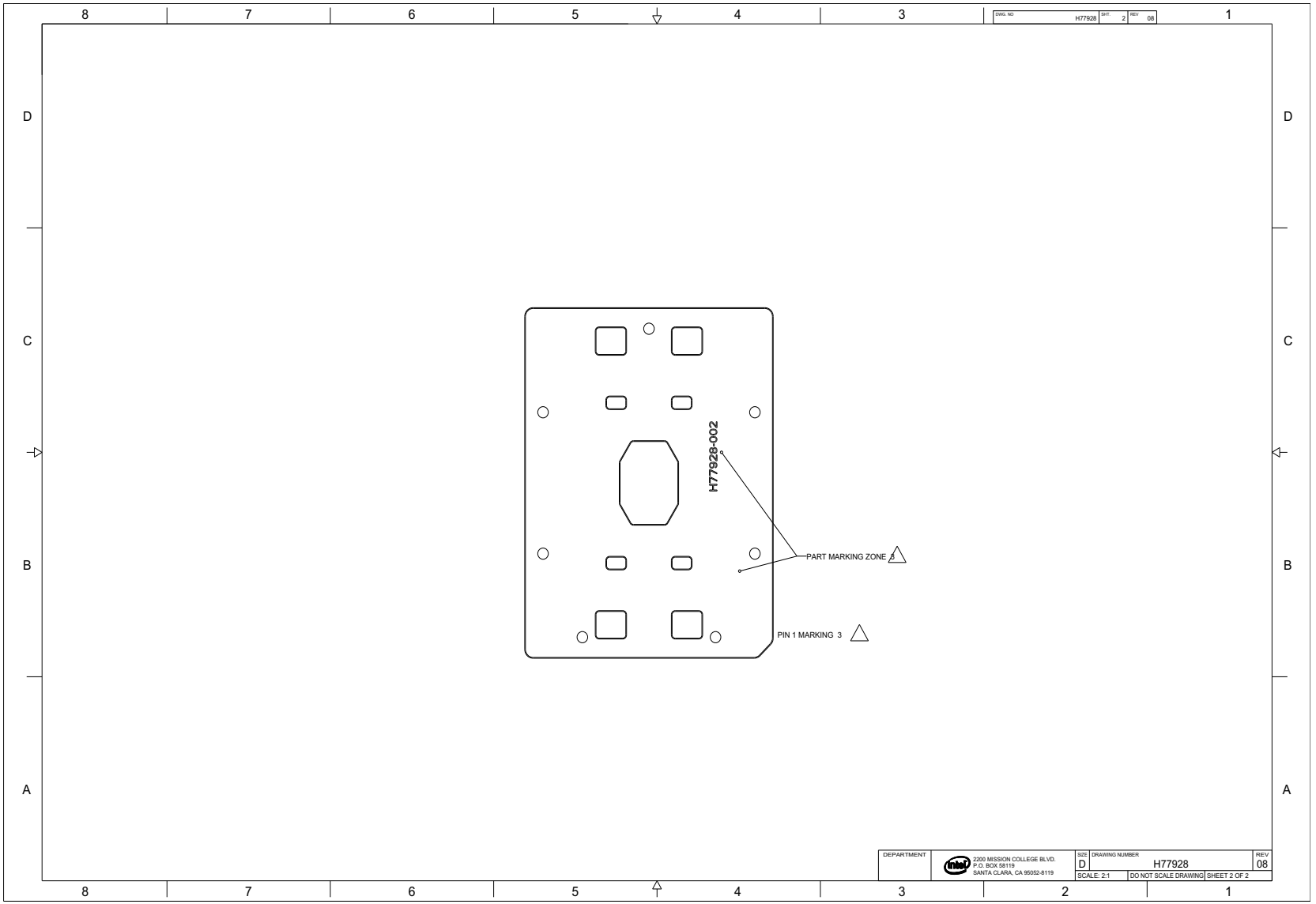


Figure D-14. Narrow Dust Cover (Sheet 1 of 2)

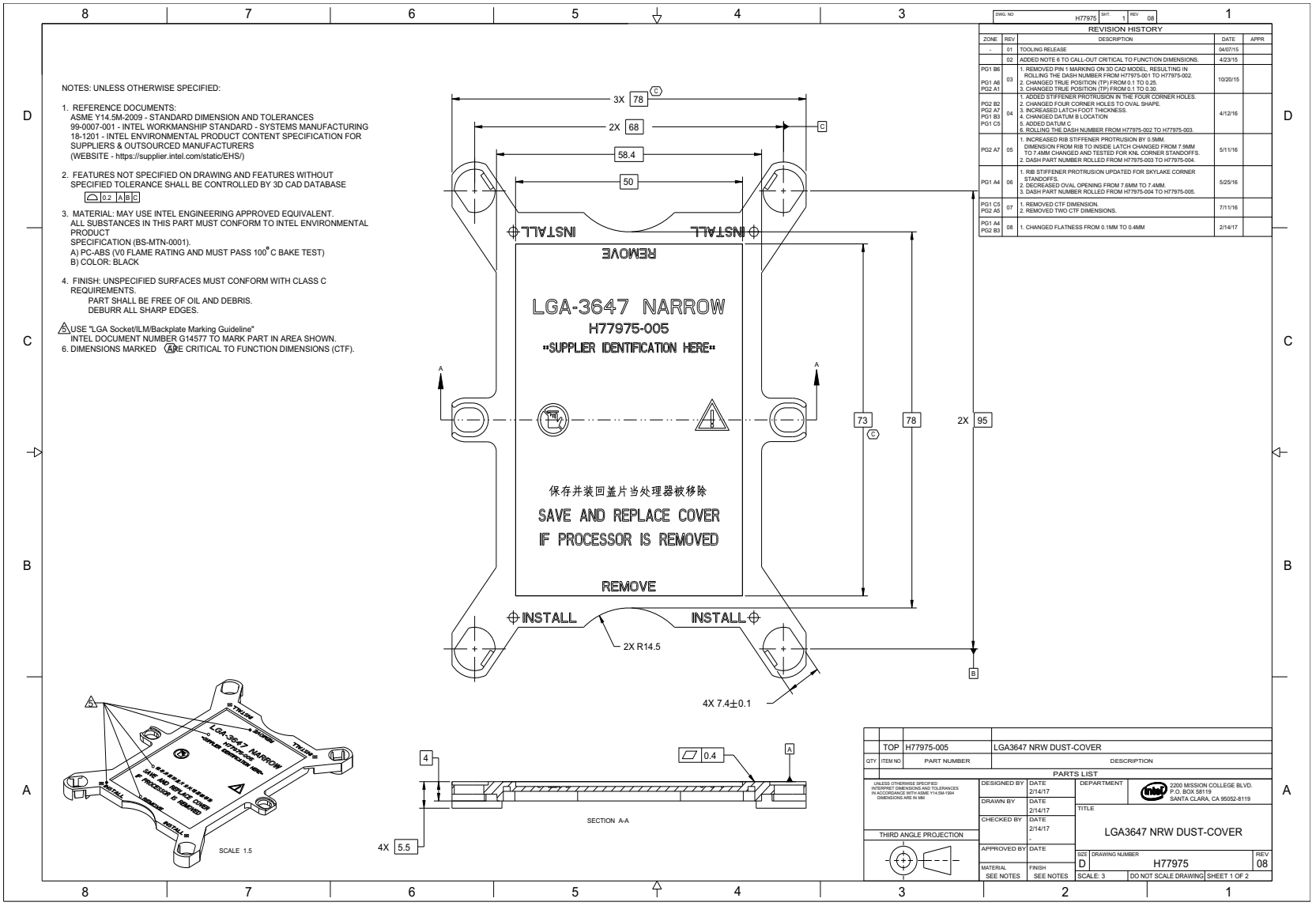


Figure D-14. Narrow Dust Cover (Sheet 2 of 2)

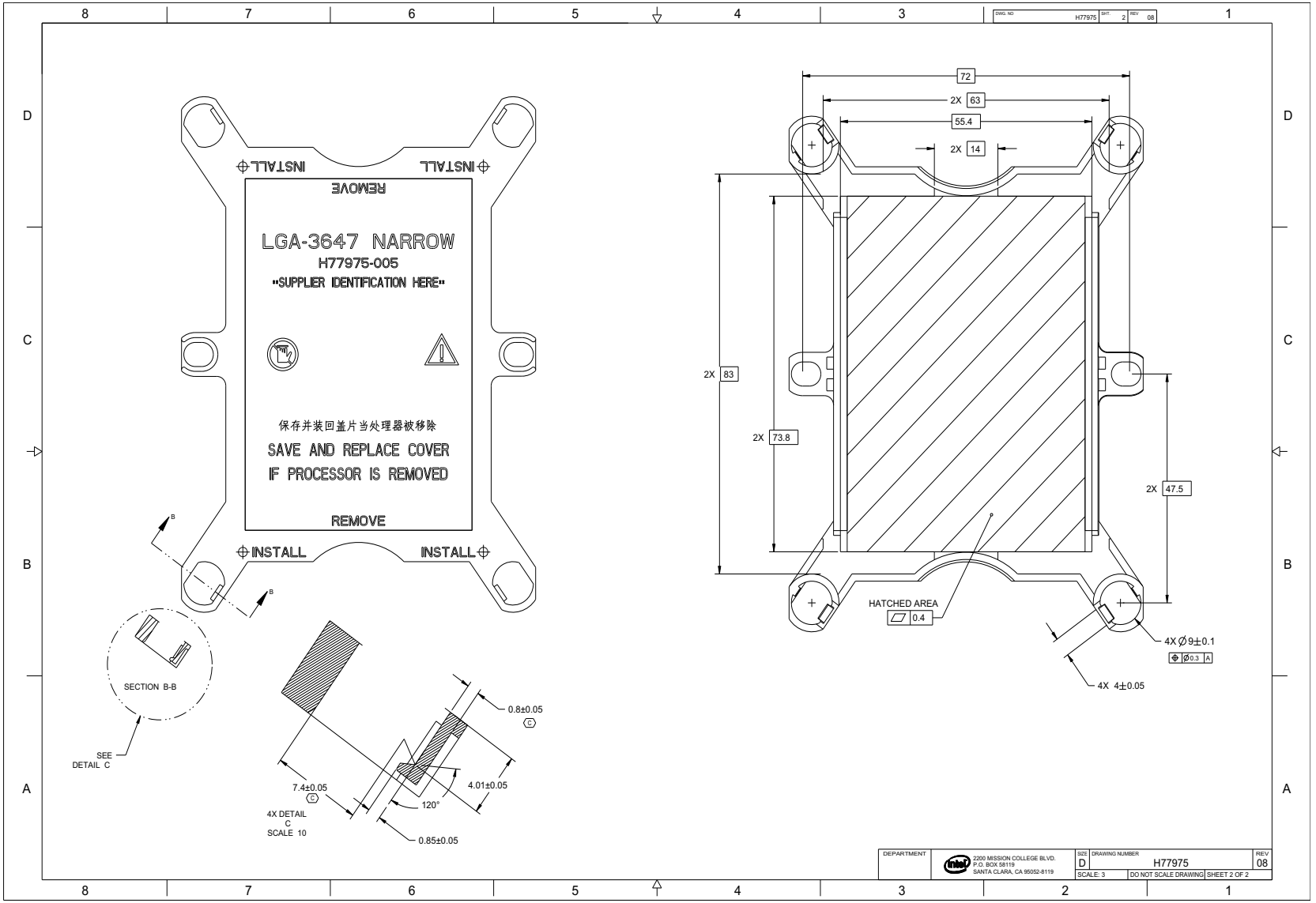


Figure D-15. Narrow Spring Assembly

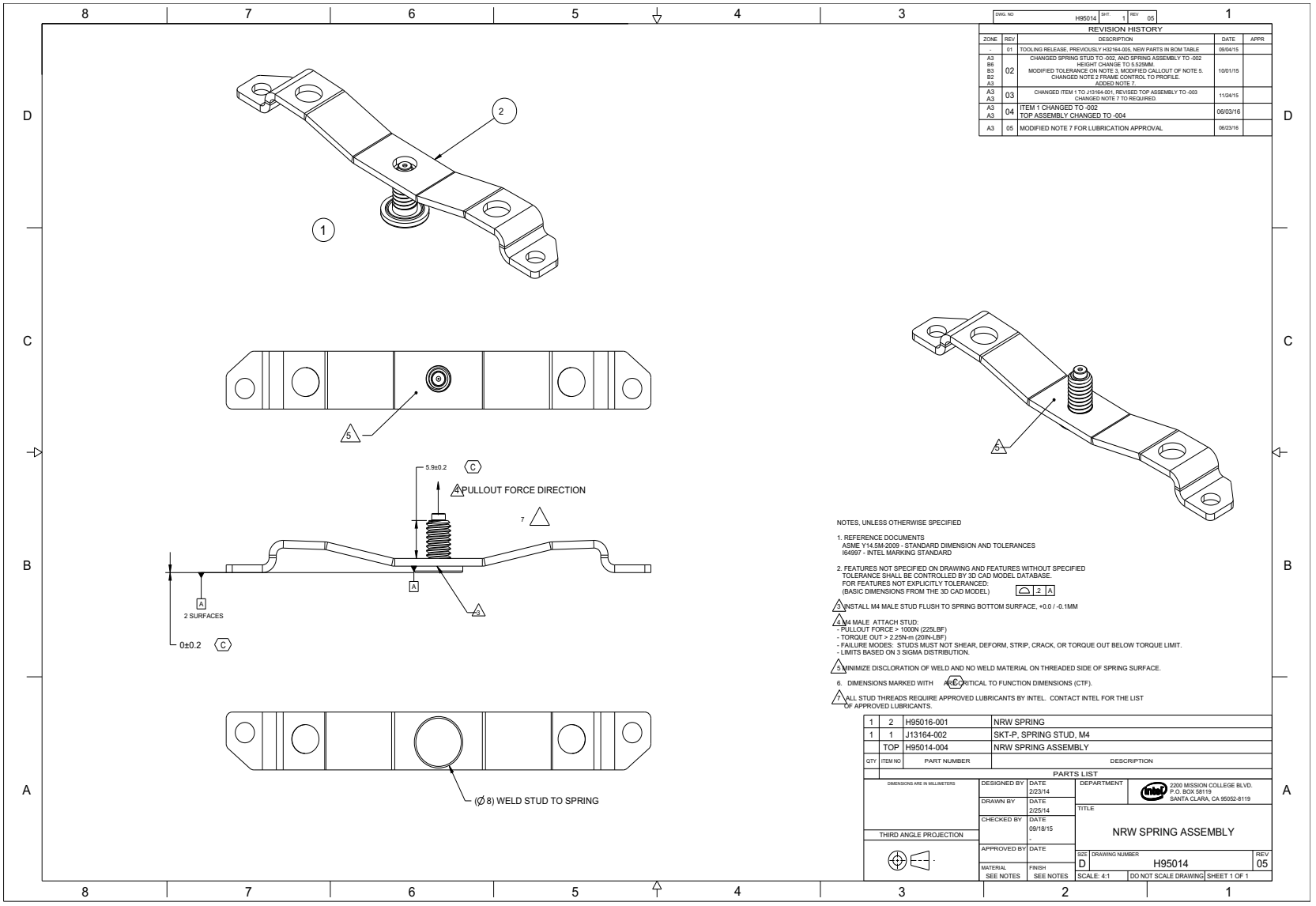


Figure D-16. Narrow Spring

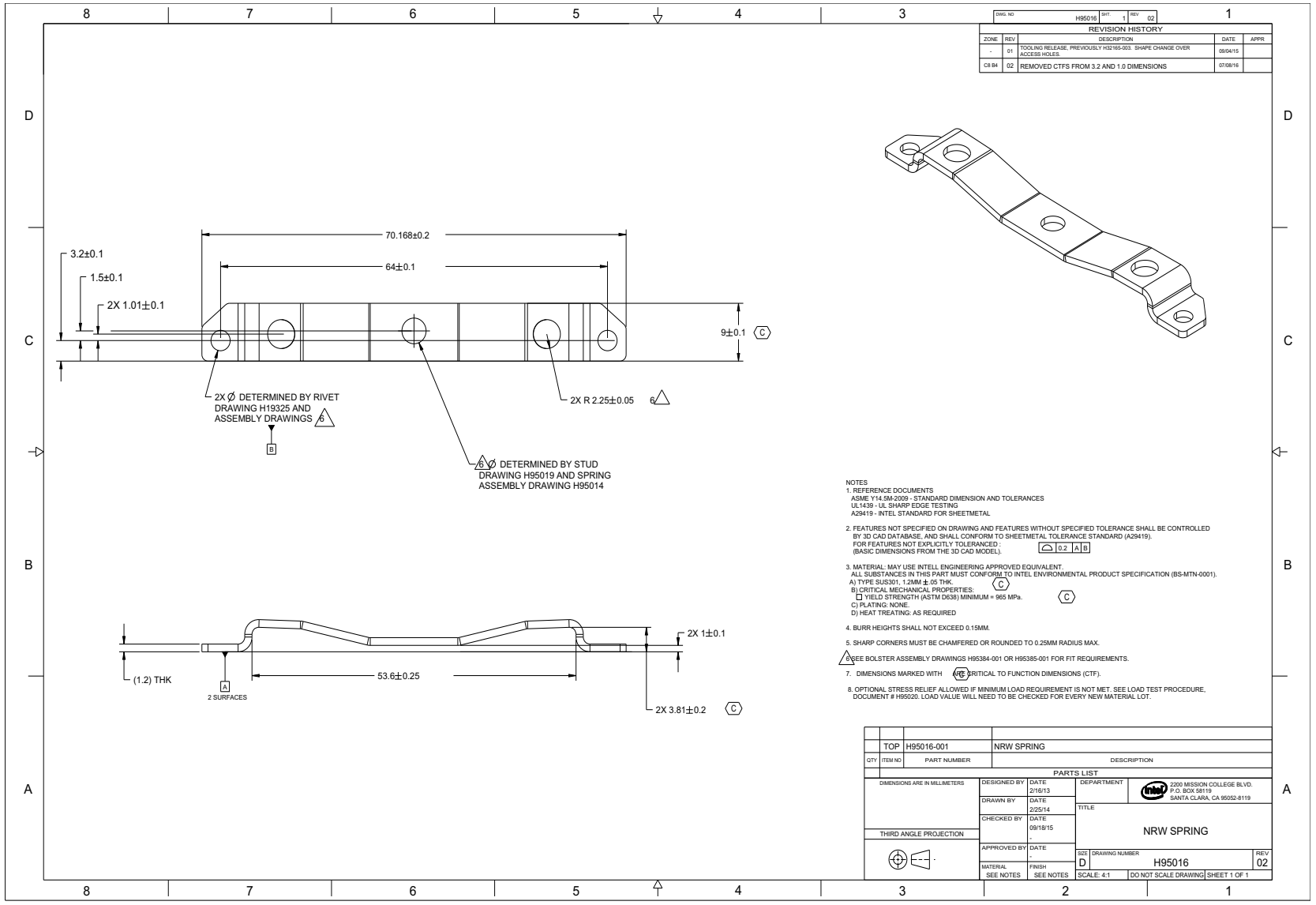
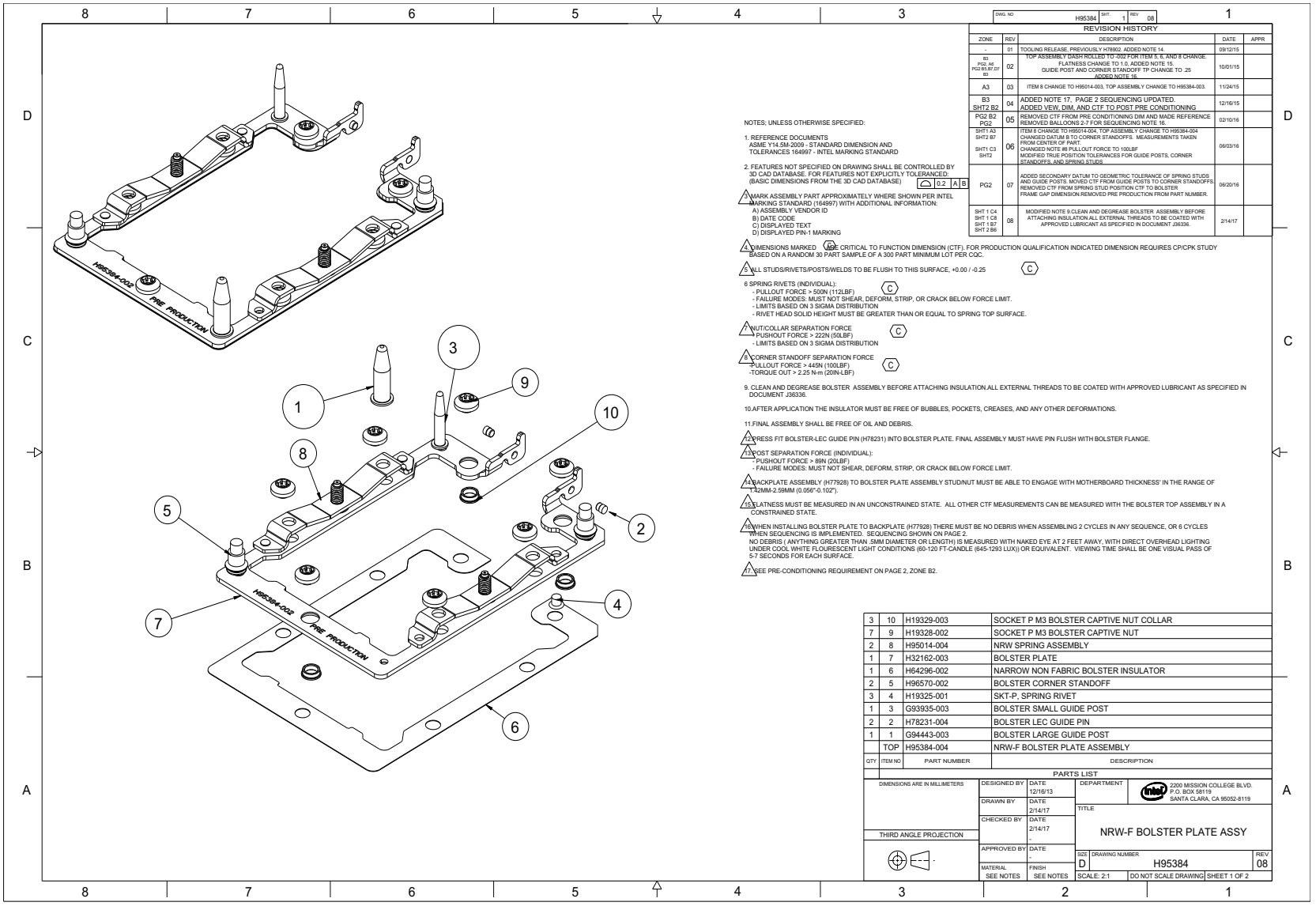


Figure D-17. Narrow - Fabric Bolster Plate Assembly (Sheet 1 of 2)



DWG. NO H95384 SHT. 1 REV 08

REVISION HISTORY

ZONE	REV	DESCRIPTION	DATE	APPR
-	01	TOOLING RELEASE, PREVIOUSLY H78902. ADDED NOTE 14.	09/12/15	
B3 PG2, A6 PG2 B5,B7,D7 B3	02	TOP ASSEMBLY DASH ROLLED TO -002 FOR ITEM 5, 6, AND 8 CHANGE: FLATNESS CHANGE TO 1.0, ADDED NOTE 15. GUIDE POST AND CORNER STANDOFF TP CHANGE TO .25 ADDED NOTE 16.	10/01/15	
A3	03	ITEM 8 CHANGE TO H95014-003, TOP ASSEMBLY CHANGE TO H95384-003.	11/24/15	
B3 SHT2 B2	04	ADDED NOTE 17, PAGE 2 SEQUENCING UPDATED. ADDED VEW, DIM, AND CTF TO POST PRE CONDITIONING	12/16/15	
PG2 B2 PG2	05	REMOVED CTF FROM PRE CONDITIONING DIM AND MADE REFERENCE REMOVED BALLOONS 2-7 FOR SEQUENCING NOTE 16.	02/10/16	
SHT1 A3 SHT2 B7 SHT1 C3 SHT2	06	ITEM 8 CHANGE TO H95014-004, TOP ASSEMBLY CHANGE TO H95384-004 CHANGED DATUM B TO CORNER STANDOFFS. MEASUREMENTS TAKEN FROM CENTER OF PART. CHANGED NOTE #8 PULLOUT FORCE TO 100LBF MODIFIED TRUE POSITION TOLERANCES FOR GUIDE POSTS, CORNER STANDOFFS, AND SPRING STUDS	06/03/16	
PG2	07	ADDED SECONDARY DATUM TO GEOMETRIC TOLERANCE OF SPRING STUDS AND GUIDE POSTS. MOVED CTF FROM GUIDE POSTS TO CORNER STANDOFFS. REMOVED CTF FROM SPRING STUD POSITION CTF TO BOLSTER FRAME GAP DIMENSION.REMOVED PRE PRODUCTION FROM PART NUMBER.	06/20/16	
SHT 1 C4 SHT 1 C8 SHT 1 B7 SHT 2 B6	08	MODIFIED NOTE 9.CLEAN AND DEGREASE BOLSTER ASSEMBLY BEFORE ATTACHING INSULATION.ALL EXTERNAL THREADS TO BE COATED WITH APPROVED LUBRICANT AS SPECIFIED IN DOCUMENT J36336.	2/14/17	

NOTES; UNLESS OTHERWISE SPECIFIED:

1. REFERENCE DOCUMENTS
ASME Y14.5M-2009 - STANDARD DIMENSION AND TOLERANCES 164997 - INTEL MARKING STANDARD

2. FEATURES NOT SPECIFIED ON DRAWING SHALL BE CONTROLLED BY 3D CAD DATABASE. FOR FEATURES NOT EXPLICITLY TOLERANCED: (BASIC DIMENSIONS FROM THE 3D CAD DATABASE) ⌓ 0.2 A B

3 MARK ASSEMBLY PART APPROXIMATELY WHERE SHOWN PER INTEL MARKING STANDARD (164997) WITH ADDITIONAL INFORMATION:
A) ASSEMBLY VENDOR ID
B) DATE CODE
C) DISPLAYED TEXT
D) DISPLAYED PIN-1 MARKING

4 DIMENSIONS MARKED (C) ARE CRITICAL TO FUNCTION DIMENSION (CTF). FOR PRODUCTION QUALIFICATION INDICATED DIMENSION REQUIRES CP/CPK STUDY BASED ON A RANDOM 30 PART SAMPLE OF A 300 PART MINIMUM LOT PER CQC.

5 ALL STUDS/RIVETS/POSTS/WELDS TO BE FLUSH TO THIS SURFACE, +0.00 / -0.25 (C)

6 SPRING RIVETS (INDIVIDUAL): (C)
- PULLOUT FORCE > 500N (112LBF)
- FAILURE MODES: MUST NOT SHEAR, DEFORM, STRIP, OR CRACK BELOW FORCE LIMIT.
- LIMITS BASED ON 3 SIGMA DISTRIBUTION
- RIVET HEAD SOLID HEIGHT MUST BE GREATER THAN OR EQUAL TO SPRING TOP SURFACE.

7 NUT/COLLAR SEPARATION FORCE (C)
PUSHOUT FORCE > 222N (50LBF)
- LIMITS BASED ON 3 SIGMA DISTRIBUTION

8 CORNER STANDOFF SEPARATION FORCE (C)
PULLOUT FORCE > 445N (100LBF)
-TORQUE OUT > 2.25 N-m (20IN-LBF)

9. CLEAN AND DEGREASE BOLSTER ASSEMBLY BEFORE ATTACHING INSULATION.ALL EXTERNAL THREADS TO BE COATED WITH APPROVED LUBRICANT AS SPECIFIED IN DOCUMENT J36336.

10.AFTER APPLICATION THE INSULATOR MUST BE FREE OF BUBBLES, POCKETS, CREASES, AND ANY OTHER DEFORMATIONS.

11.FINAL ASSEMBLY SHALL BE FREE OF OIL AND DEBRIS.

12 PRESS FIT BOLSTER-LEC GUIDE PIN (H78231) INTO BOLSTER PLATE. FINAL ASSEMBLY MUST HAVE PIN FLUSH WITH BOLSTER FLANGE.

13 POST SEPARATION FORCE (INDIVIDUAL):
PUSHOUT FORCE > 89N (20LBF)
- FAILURE MODES: MUST NOT SHEAR, DEFORM, STRIP, OR CRACK BELOW FORCE LIMIT.

14 BACKPLATE ASSEMBLY (H77928) TO BOLSTER PLATE ASSEMBLY STUD/NUT MUST BE ABLE TO ENGAGE WITH MOTHERBOARD THICKNESS' IN THE RANGE OF 1.42MM-2.59MM (0.056"-0.102").

15 FLATNESS MUST BE MEASURED IN AN UNCONSTRAINED STATE. ALL OTHER CTF MEASUREMENTS CAN BE MEASURED WITH THE BOLSTER TOP ASSEMBLY IN A CONSTRAINED STATE.

16 WHEN INSTALLING BOLSTER PLATE TO BACKPLATE (H77928) THERE MUST BE NO DEBRIS WHEN ASSEMBLING 2 CYCLES IN ANY SEQUENCE, OR 6 CYCLES WHEN SEQUENCING IS IMPLEMENTED. SEQUENCING SHOWN ON PAGE 2.
NO DEBRIS (ANYTHING GREATER THAN .5MM DIAMETER OR LENGTH) IS MEASURED WITH NAKED EYE AT 2 FEET AWAY, WITH DIRECT OVERHEAD LIGHTING UNDER COOL WHITE FLOURESCENT LIGHT CONDITIONS (60-120 FT-CANDLE (645-1293 LUX)) OR EQUIVALENT. VIEWING TIME SHALL BE ONE VISUAL PASS OF 5-7 SECONDS FOR EACH SURFACE.

17 SEE PRE-CONDITIONING REQUIREMENT ON PAGE 2, ZONE B2.

QTY	ITEM NO	PART NUMBER	DESCRIPTION
3	10	H19329-003	SOCKET P M3 BOLSTER CAPTIVE NUT COLLAR
7	9	H19328-002	SOCKET P M3 BOLSTER CAPTIVE NUT
2	8	H95014-004	NRW SPRING ASSEMBLY
1	7	H32162-003	BOLSTER PLATE
1	6	H64296-002	NARROW NON FABRIC BOLSTER INSULATOR
2	5	H96570-002	BOLSTER CORNER STANDOFF
3	4	H19325-001	SKT-P, SPRING RIVET
1	3	G93935-003	BOLSTER SMALL GUIDE POST
2	2	H78231-004	BOLSTER LEC GUIDE PIN
1	1	G94443-003	BOLSTER LARGE GUIDE POST
	TOP	H95384-004	NRW-F BOLSTER PLATE ASSEMBLY

PARTS LIST

DIMENSIONS ARE IN MILLIMETERS
THIRD ANGLE PROJECTION

DESIGNED BY	DATE	12/16/13
DRAWN BY	DATE	2/14/17
CHECKED BY	DATE	2/14/17
APPROVED BY	DATE	-
MATERIAL	FINISH	
SEE NOTES	SEE NOTES	

DEPARTMENT
2200 MISSION COLLEGE BLVD.
P.O. BOX 58119
SANTA CLARA, CA 95052-8119

TITLE
NRW-F BOLSTER PLATE ASSY

SIZE	DRAWING NUMBER	REV
D	H95384	08

SCALE: 2:1 | DO NOT SCALE DRAWING | SHEET 1 OF 2

Figure D-17. Narrow - Fabric Bolster Plate Assembly (Sheet 2 of 2)

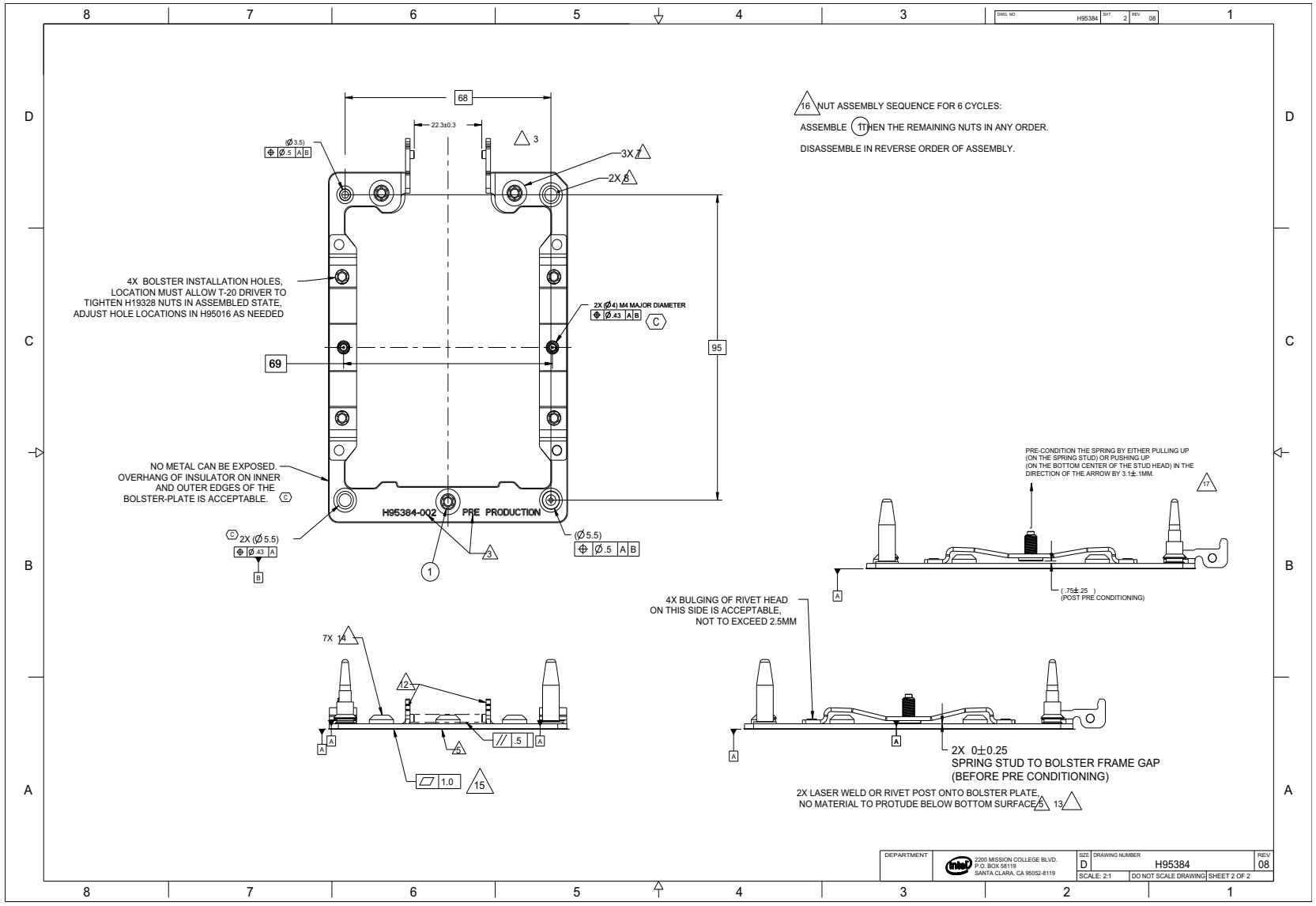


Figure D-18. Narrow Bolster Plate Assembly (Sheet 1 of 2)

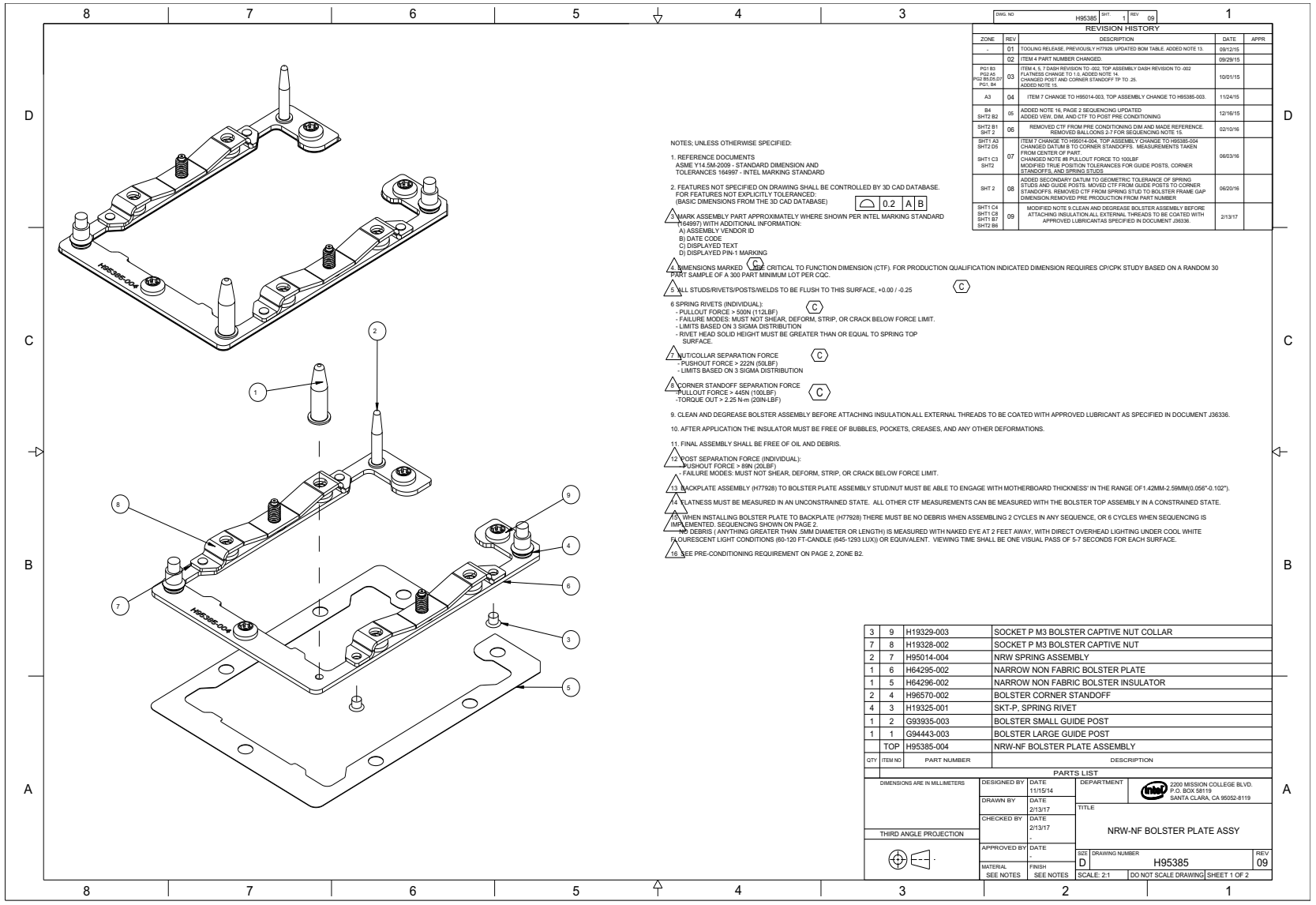


Figure D-18. Narrow Bolster Plate Assembly (Sheet 2 of 2)

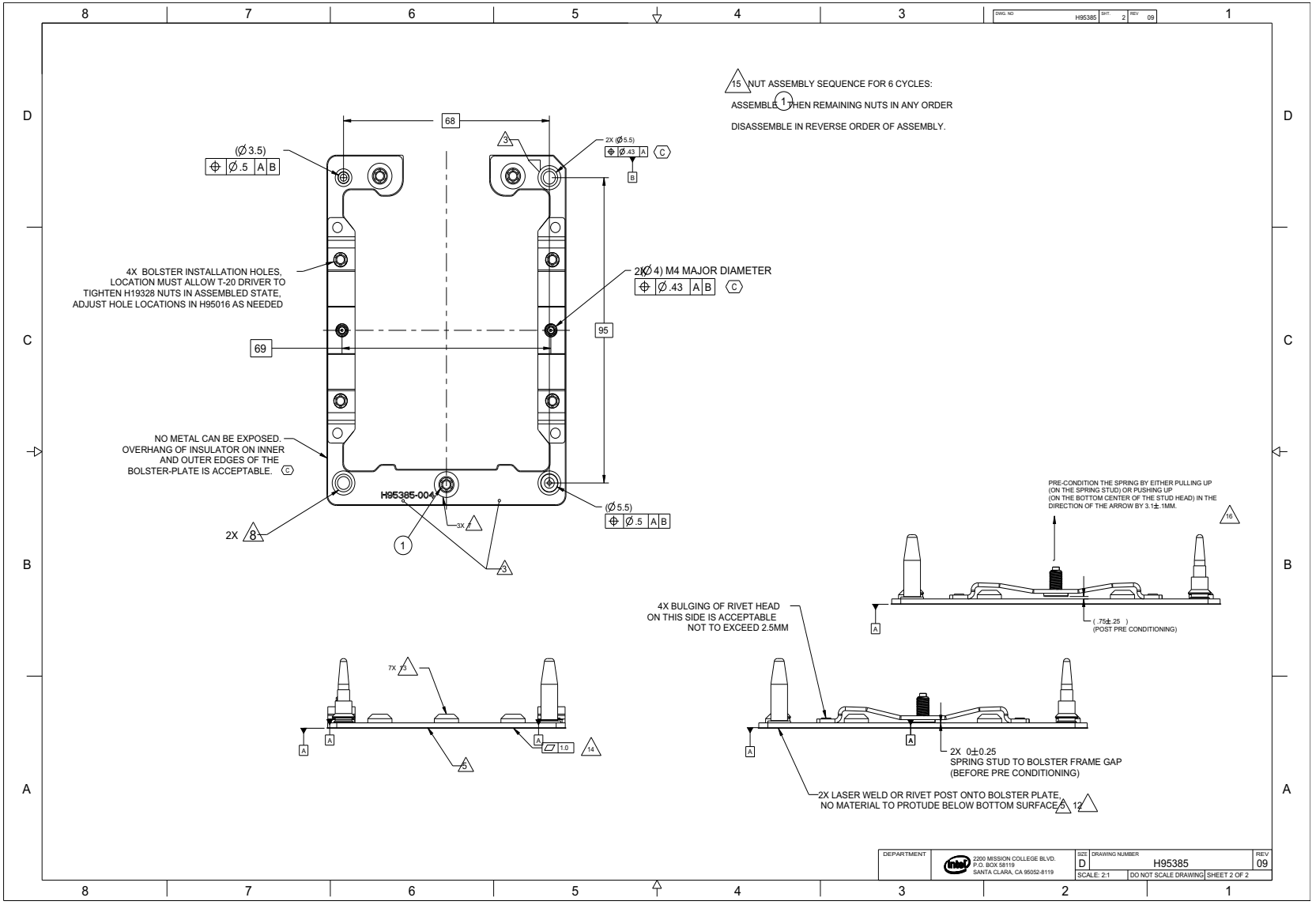


Figure D-19. Bolster Corner Standoff

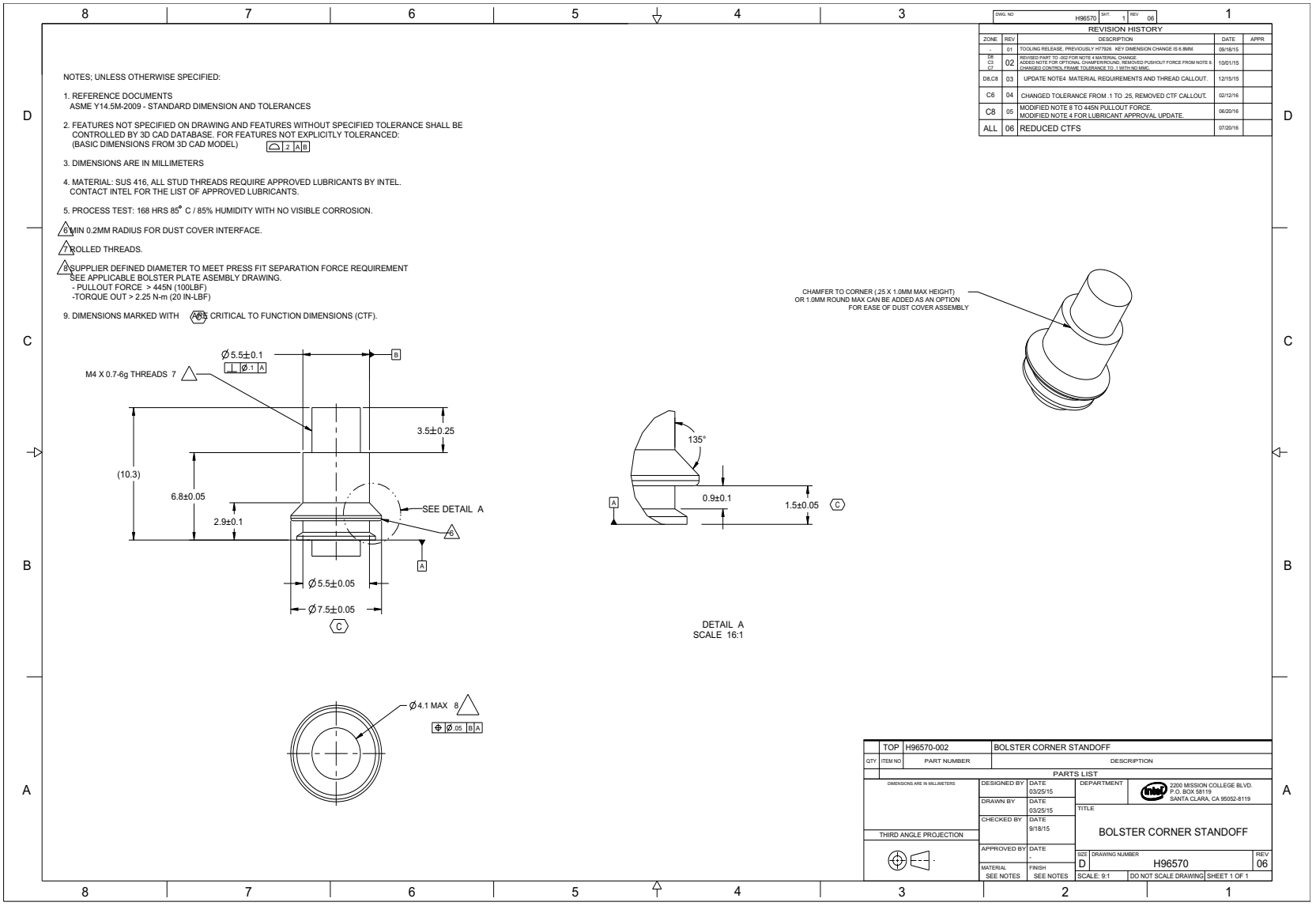


Figure D-20. Narrow Spring Stud

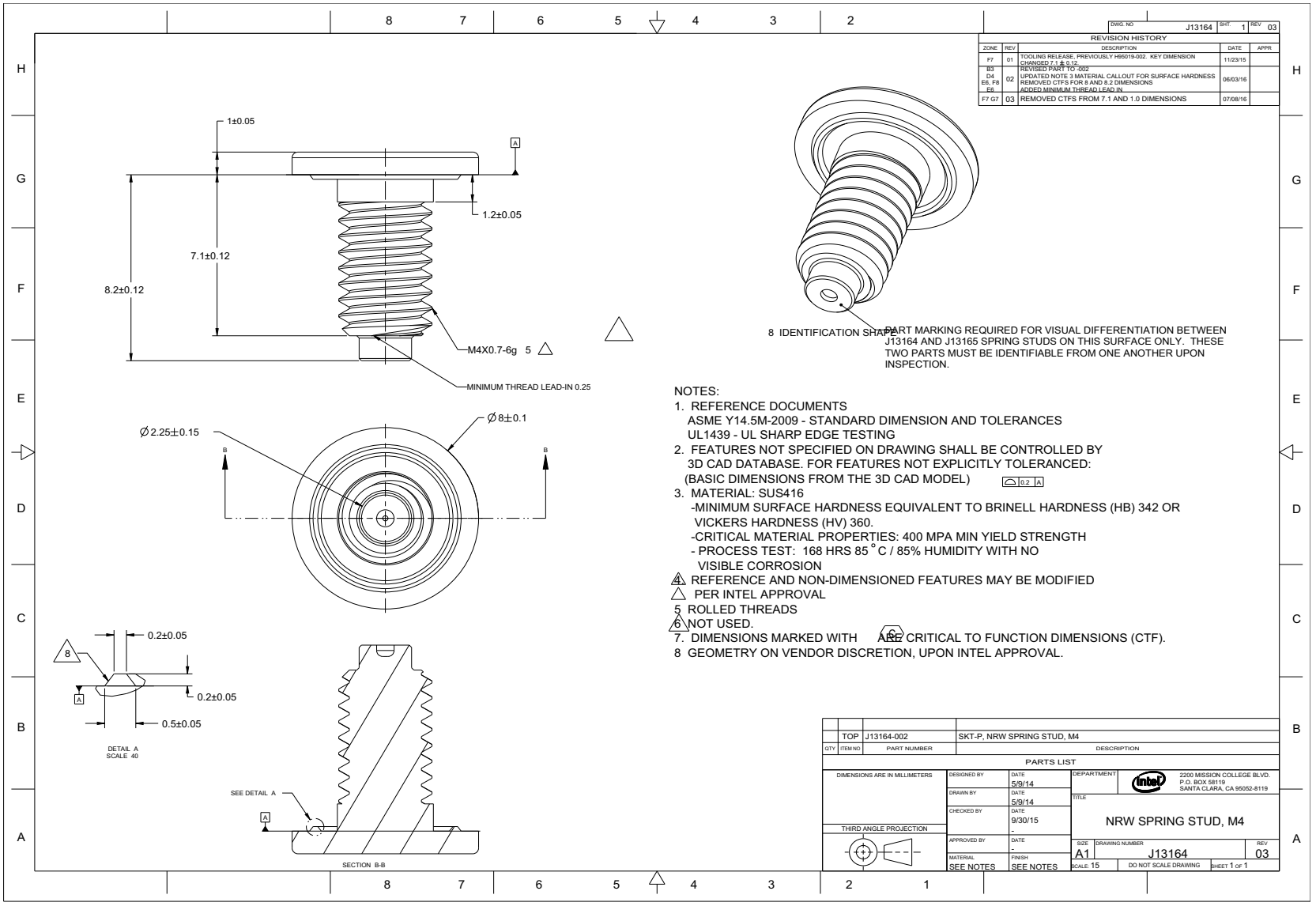


Figure D-21. Backplate Stud: Long

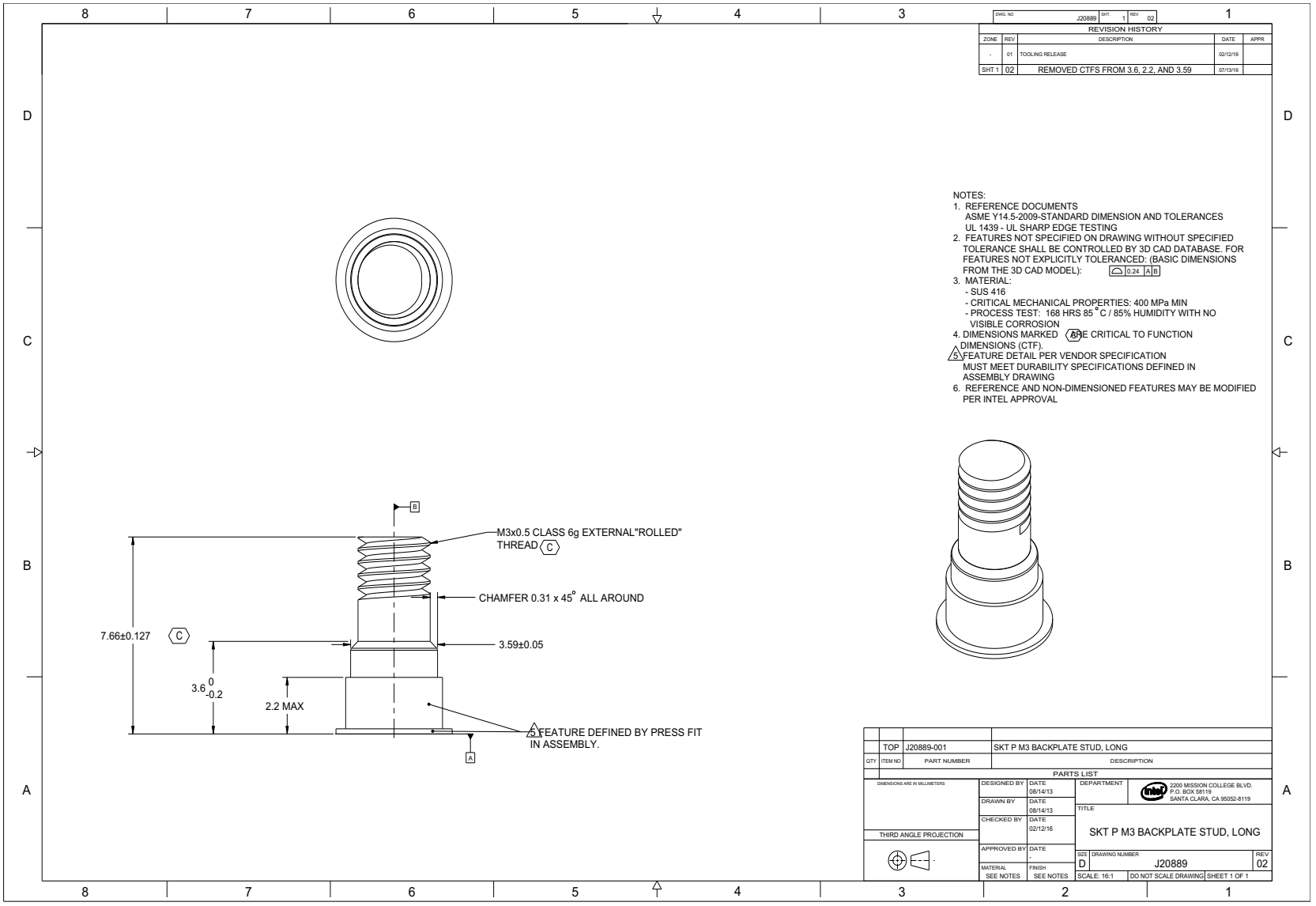


Figure D-22. Narrow Backplate Long Stud Assembly (Sheet 1 of 2)

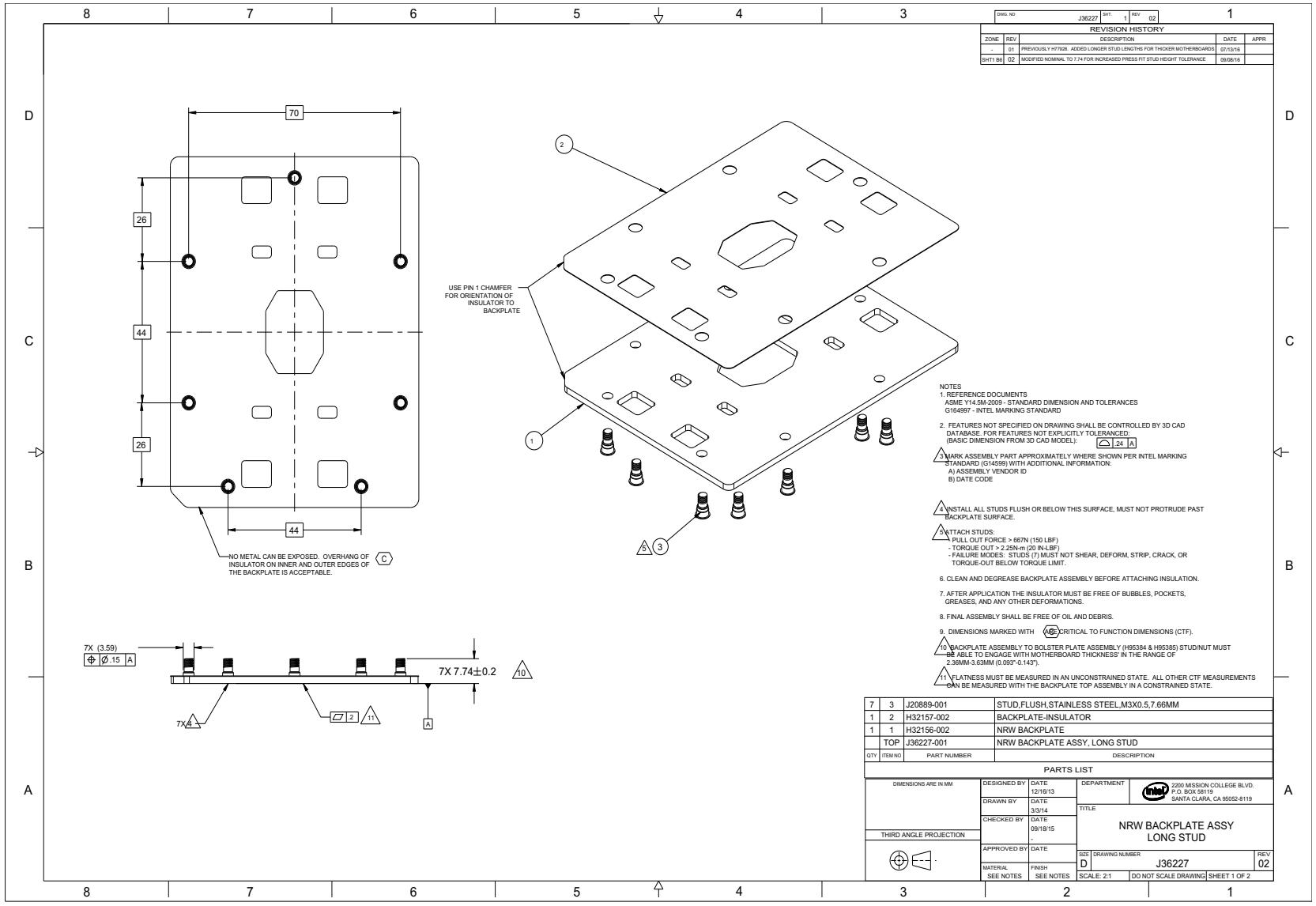
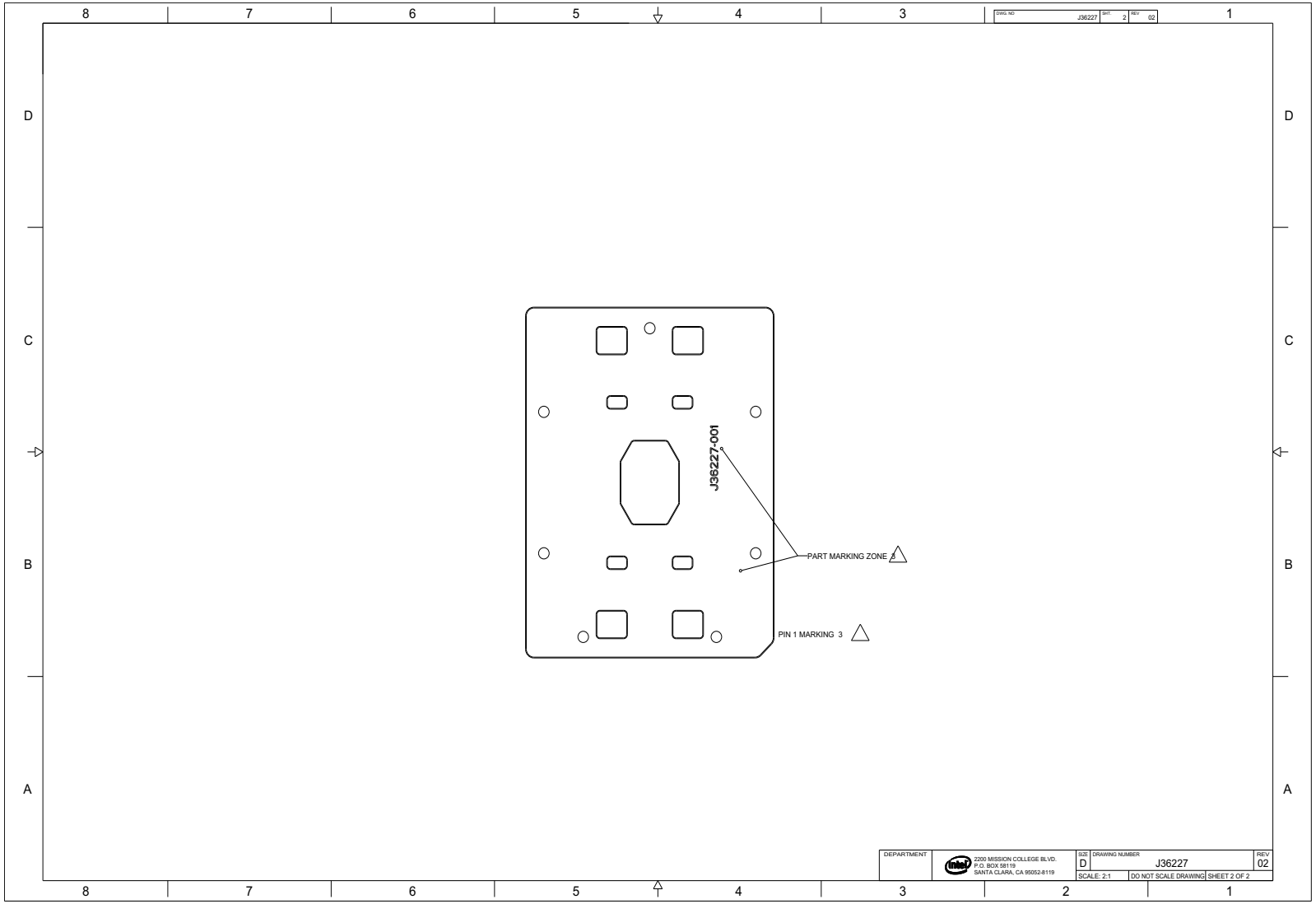


Figure D-22. Narrow Backplate Long Stud Assembly (Sheet 2 of 2)



§

E Heatsink Mechanical Drawings

E.1 Heatsink Drawings

Table E-1 lists the reference heatsink mechanical drawings that are used in the Second Generation Intel® Xeon® Scalable Processors based platform.

Table E-1. Heatsink Drawings List

Description	Figure
2U Heatsink Assembly	Figure E-1
2U Heatsink Heatpipe: Small	Figure E-2
2U Heatsink Heatpipe: Large	Figure E-3
2U Heatsink Copper Slug	Figure E-4
2U Heatsink Aluminum Base	Figure E-5
2U Heatsink Fin Assembly	Figure E-6
Delrin Heatsink Washer	Figure E-7
TIM PCM45F	Figure E-8
1U Heatsink Assembly	Figure E-9
1U Heatsink	Figure E-10
1U Extruded Heatsink Assembly	Figure E-11
1U Extruded Heatsink	Figure E-12
Heatsink Label	Figure E-13
Heatsink Collar	Figure E-14
Heatsink Nut	Figure E-15
Extruded Aluminum Heatsink Label	Figure E-16

E.2 1U Copper Base Heatsink Drawings

Table E-2 lists the mechanical drawings that compose the 1U Copper Base heatsink configuration.

Table E-2. 1U Copper Base Heatsink Drawing List

Description	Figure
1U Heatsink Assembly	Figure E-9
• Delrin Heatsink Washer	Figure E-7
• TIM PCM45F	Figure E-8
• 1U Heatsink	Figure E-10
• Heatsink Label	Figure E-13
• Heatsink Collar	Figure E-14
• Heatsink Nut	Figure E-15

E.3 1U Extruded Aluminum Heatsink Drawings

Table E-3 lists the mechanical drawings that compose the 1U Extruded Aluminum heatsink configuration.

Table E-3. 1U Extruded Aluminum Heatsink Drawing List

Description	Figure
1U Extruded Heatsink Assembly	Figure E-11
• Delrin Heatsink Washer	Figure E-7
• TIM PCM45F	Figure E-8
• 1U Extruded Heatsink	Figure E-12
• Heatsink Collar	Figure E-14
• Heatsink Nut	Figure E-15
• Extruded Aluminum Heatsink Label	Figure E-16

E.4 2U Passive Heatsink Drawing

Table E-4 lists the mechanical drawings that compose the 2U Passive heatsink configuration.

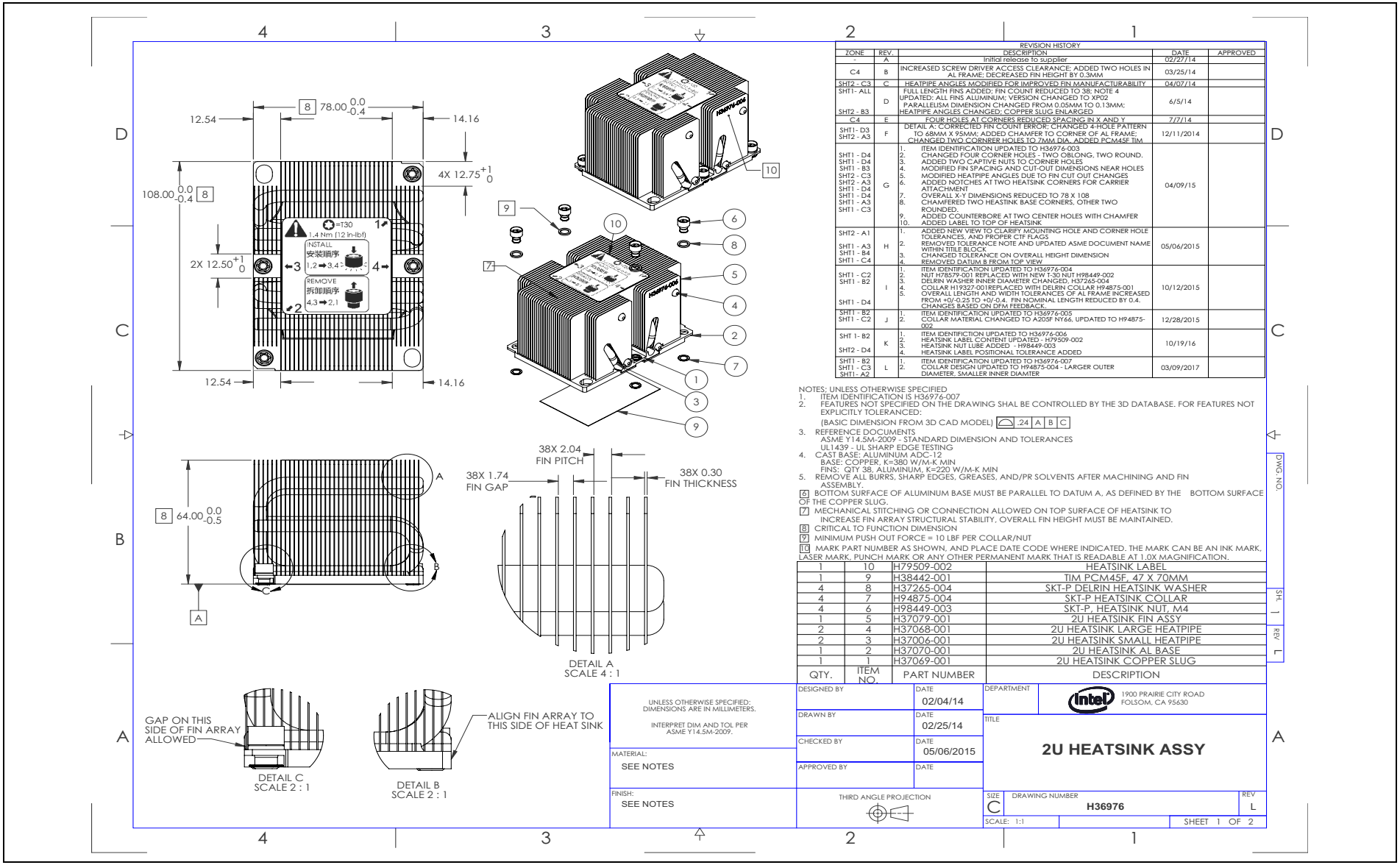
Table E-4. 2U Passive Heatsink Drawing List (Sheet 1 of 2)

Description	Figure
2U Heatsink Assembly	Figure E-1
• 2U Heatsink Heatpipe: Small	Figure E-2
• 2U Heatsink Heatpipe: Large	Figure E-3
• 2U Heatsink Copper Slug	Figure E-4
• 2U Heatsink Aluminum Base	Figure E-5
• 2U Heatsink Fin Assembly	Figure E-6
• Delrin Heatsink Washer	Figure E-7
• TIM PCM45F	Figure E-8

Table E-4. 2U Passive Heatsink Drawing List (Sheet 2 of 2)

Description	Figure
• Heatsink Label	Figure E-13
• Heatsink Collar	Figure E-14
• Heatsink Nut	Figure E-15

Figure E-1. 2U Heatsink Assembly (Sheet 1 of 2)



REVISION HISTORY				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
-	A	Initial release to supplier	02/27/14	
C4	B	INCREASED SCREW DRIVER ACCESS CLEARANCE; ADDED TWO HOLES IN AL FRAME; DECREASED FIN HEIGHT BY 0.3MM	03/25/14	
SHT2 - C3	C	HEATPIPE ANGLES MODIFIED FOR IMPROVED FIN MANUFACTURABILITY	04/07/14	
SHT1- ALL SHT2 - B3	D	FULL LENGTH FINS ADDED; FIN COUNT REDUCED TO 38; NOTE 4 UPDATED; ALL FINS ALUMINUM; VERSION CHANGED TO XP02 PARALLELISM DIMENSION CHANGED FROM 0.05MM TO 0.13MM; HEATPIPE ANGLES CHANGED; COPPER SLUG ENLARGED	6/5/14	
C4	E	FOUR HOLES AT CORNERS REDUCED SPACING IN X AND Y	7/7/14	
SHT1- D3 SHT2 - A3	F	DETAIL A: CORRECTED FIN COUNT ERROR; CHANGED 4-HOLE PATTERN TO 68MM X 95MM; ADDED CHAMFER TO CORNER OF AL FRAME; CHANGED TWO CORNRER HOLES TO 7MM DIA. ADDED PCM45F TIM	12/11/2014	
SHT1 - D4 SHT1 - D4 SHT1 - B3 SHT2 - C3 SHT2 - A3 SHT1 - D4 SHT1 - D4 SHT1 - A3 SHT1 - C3	G	1. ITEM IDENTIFICATION UPDATED TO H36976-003 2. CHANGED FOUR CORNER HOLES - TWO OBLONG, TWO ROUND. 3. ADDED TWO CAPTIVE NUTS TO CORNER HOLES 4. MODIFIED FIN SPACING AND CUT-OUT DIMENSIONS NEAR HOLES 5. MODIFIED HEATPIPE ANGLES DUE TO FIN CUT OUT CHANGES 6. ADDED NOTCHES AT TWO HEATSINK CORNERS FOR CARRIER ATTACHMENT 7. OVERALL X-Y DIMENSIONS REDUCED TO 78 X 108 8. CHAMFERED TWO HEASTINK BASE CORNERS, OTHER TWO ROUNDED. 9. ADDED COUNTERBORE AT TWO CENTER HOLES WITH CHAMFER 10. ADDED LABEL TO TOP OF HEATSINK	04/09/15	
SHT2 - A1 SHT1 - A3 SHT1 - B4 SHT1 - C4	H	1. ADDED NEW VIEW TO CLARIFY MOUNTING HOLE AND CORNER HOLE TOLERANCES, AND PROPER CTF FLAGS 2. REMOVED TOLERANCE NOTE AND UPDATED ASME DOCUMENT NAME WITHIN TITLE BLOCK 3. CHANGED TOLERANCE ON OVERALL HEIGHT DIMENSION 4. REMOVED DATUM B FROM TOP VIEW	05/06/2015	
SHT1 - C2 SHT1 - B2 SHT1 - D4	I	1. ITEM IDENTIFICATION UPDATED TO H36976-004 2. NUT H78579-001 REPLACED WITH NEW T-30 NUT H98449-002 3. DELRIN WASHER INNER DIAMETER CHANGED, H37265-004 4. COLLAR H19327-001REPLACED WITH DELRIN COLLAR H94875-001 5. OVERALL LENGTH AND WIDTH TOLERANCES OF AL FRAME INCREASED FROM +0/-0.25 TO +0/-0.4. FIN NOMINAL LENGTH REDUCED BY 0.4. CHANGES BASED ON DFM FEEDBACK.	10/12/2015	
SHT1 - B2 SHT1 - C2	J	1. ITEM IDENTIFICATION UPDATED TO H36976-005 2. COLLAR MATERIAL CHANGED TO A205F NY66, UPDATED TO H94875-002	12/28/2015	
SHT 1- B2 SHT2 - D4	K	1. ITEM IDENTIFICTION UPDATED TO H36976-006 2. HEATSINK LABEL CONTENT UPDATED - H79509-002 3. HEATSINK NUT LUBE ADDED - H98449-003 4. HEATSINK LABEL POSITIONAL TOLERANCE ADDED	10/19/16	
SHT1 - B2 SHT1 - C3 SHT1 - A2	L	1. ITEM IDENTIFICATION UPDATED TO H36976-007 2. COLLAR DESIGN UPDATED TO H94875-004 - LARGER OUTER DIAMETER, SMALLER INNER DIAMTER	03/09/2017	

NOTES; UNLESS OTHERWISE SPECIFIED
1. ITEM IDENTIFICATION IS H36976-007
2. FEATURES NOT SPECIFIED ON THE DRAWING SHAL BE CONTROLLED BY THE 3D DATABASE. FOR FEATURES NOT EXPLICITLY TOLERANCED:
   (BASIC DIMENSION FROM 3D CAD MODEL) .24 A B C
3. REFERENCE DOCUMENTS
   ASME Y14.5M-2009 - STANDARD DIMENSION AND TOLERANCES
   UL1439 - UL SHARP EDGE TESTING
4. CAST BASE: ALUMINUM ADC-12
   BASE: COPPER, K=380 W/M-K MIN
   FINS: QTY 38, ALUMINUM, K=220 W/M-K MIN
5. REMOVE ALL BURRS, SHARP EDGES, GREASES, AND/PR SOLVENTS AFTER MACHINING AND FIN ASSEMBLY.

6 BOTTOM SURFACE OF ALUMINUM BASE MUST BE PARALLEL TO DATUM A, AS DEFINED BY THE BOTTOM SURFACE OF THE COPPER SLUG.

7 MECHANICAL STITCHING OR CONNECTION ALLOWED ON TOP SURFACE OF HEATSINK TO INCREASE FIN ARRAY STRUCTURAL STABILITY, OVERALL FIN HEIGHT MUST BE MAINTAINED.

8 CRITICAL TO FUNCTION DIMENSION

9 MINIMUM PUSH OUT FORCE = 10 LBF PER COLLAR/NUT

10 MARK PART NUMBER AS SHOWN, AND PLACE DATE CODE WHERE INDICATED. THE MARK CAN BE AN INK MARK, LASER MARK, PUNCH MARK OR ANY OTHER PERMANENT MARK THAT IS READABLE AT 1.0X MAGNIFICATION.

QTY.	ITEM NO.	PART NUMBER	DESCRIPTION
1	10	H79509-002	HEATSINK LABEL
1	9	H38442-001	TIM PCM45F, 47 X 70MM
4	8	H37265-004	SKT-P DELRIN HEATSINK WASHER
4	7	H94875-004	SKT-P HEATSINK COLLAR
4	6	H98449-003	SKT-P, HEATSINK NUT, M4
1	5	H37079-001	2U HEATSINK FIN ASSY
2	4	H37068-001	2U HEATSINK LARGE HEATPIPE
2	3	H37006-001	2U HEATSINK SMALL HEATPIPE
1	2	H37070-001	2U HEATSINK AL BASE
1	1	H37069-001	2U HEATSINK COPPER SLUG

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS.
INTERPRET DIM AND TOL PER ASME Y14.5M-2009.

MATERIAL: SEE NOTES

FINISH: SEE NOTES

DESIGNED BY	DATE	02/04/14
DRAWN BY	DATE	02/25/14
CHECKED BY	DATE	05/06/2015
APPROVED BY	DATE	

THIRD ANGLE PROJECTION

DEPARTMENT

1900 PRAIRIE CITY ROAD
FOLSOM, CA 95630

TITLE: 2U HEATSINK ASSY

SIZE C | DRAWING NUMBER H36976 | REV L

SCALE: 1:1 | SHEET 1 OF 2

DWG NO. | SH. 1 | REV L

Figure E-1. 2U Heatsink Assembly (Sheet 2 of 2)

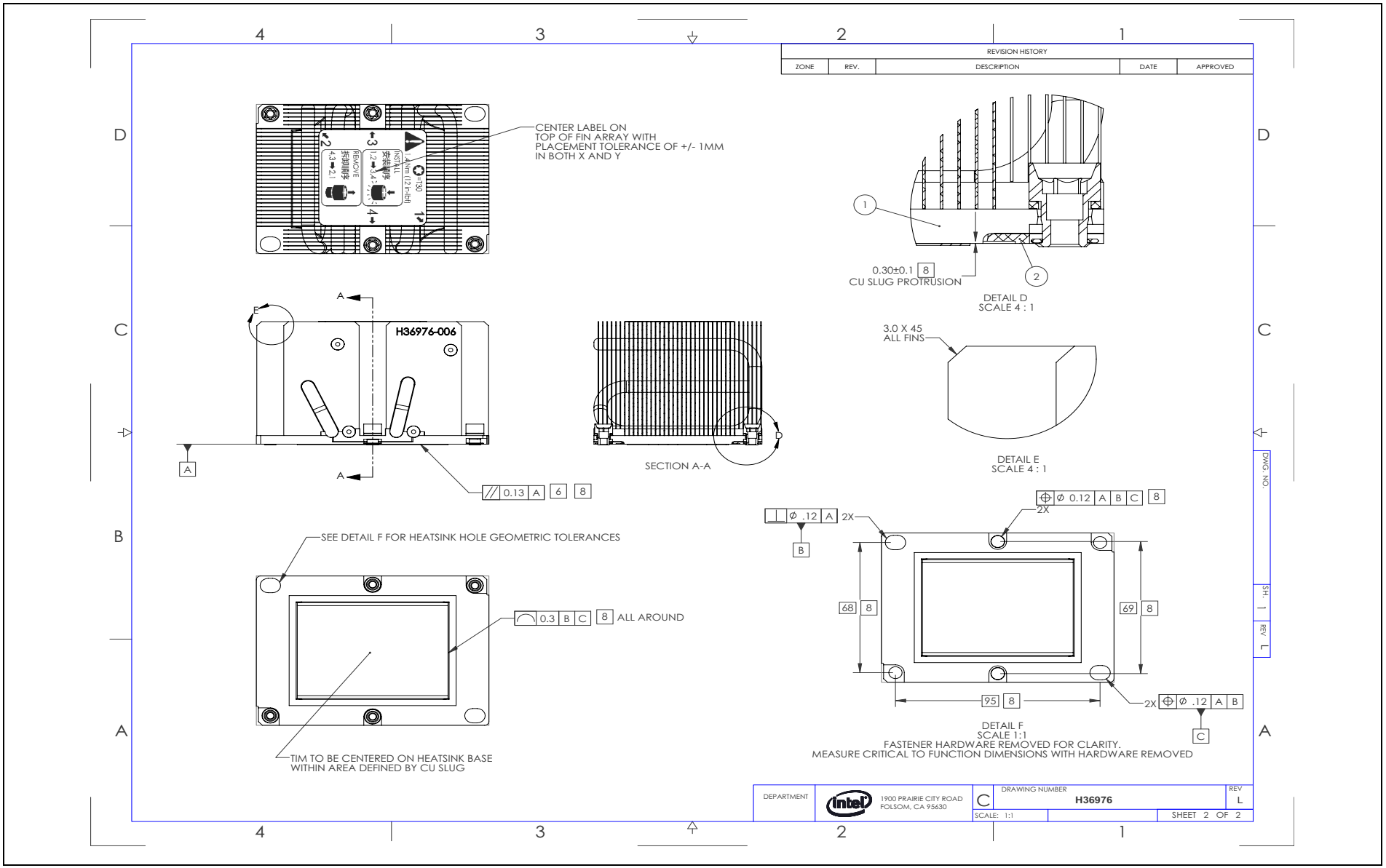


Figure E-2. 2U Heatsink Heatpipe: Small

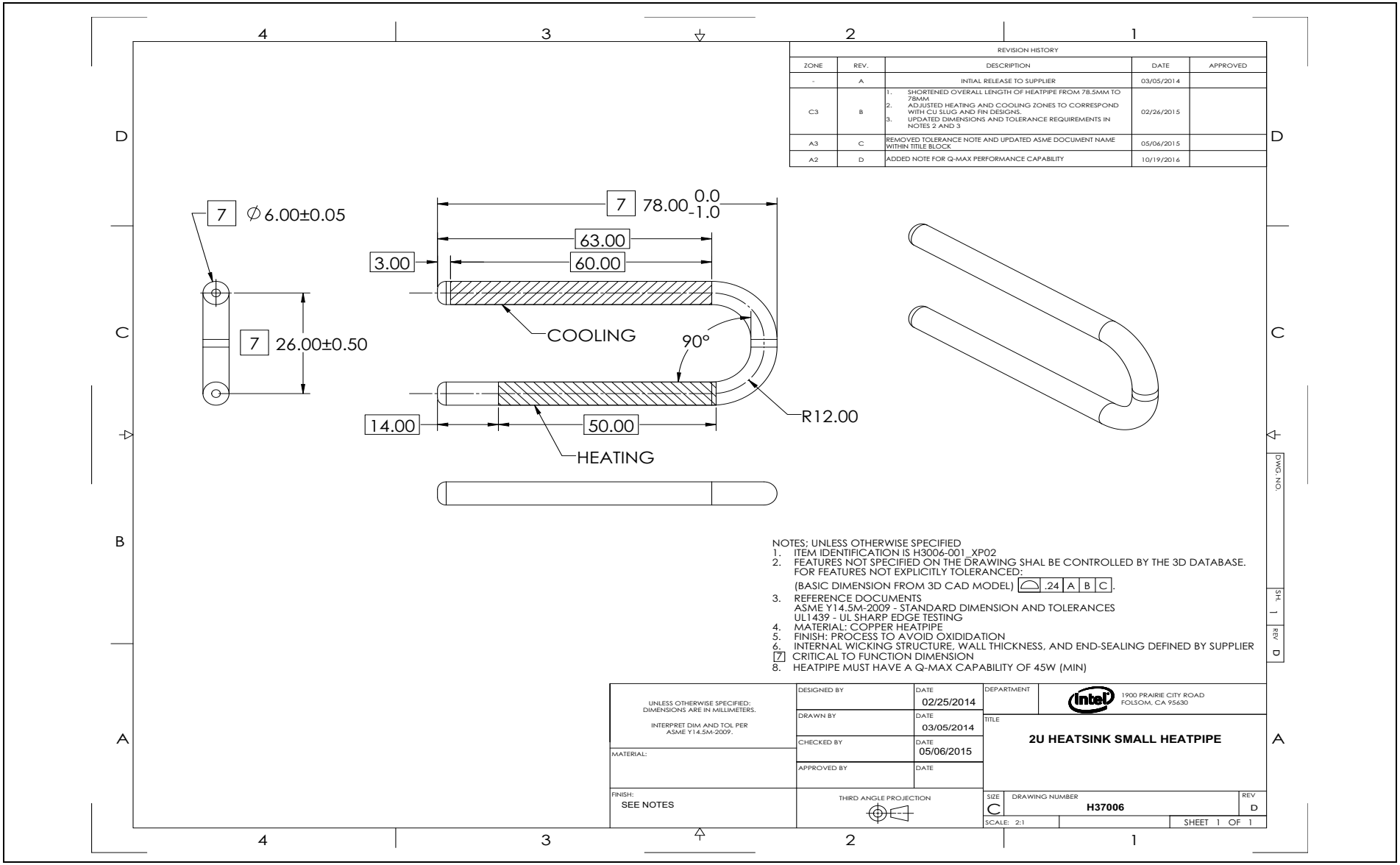


Figure E-3. 2U Heatsink Heatpipe: Large

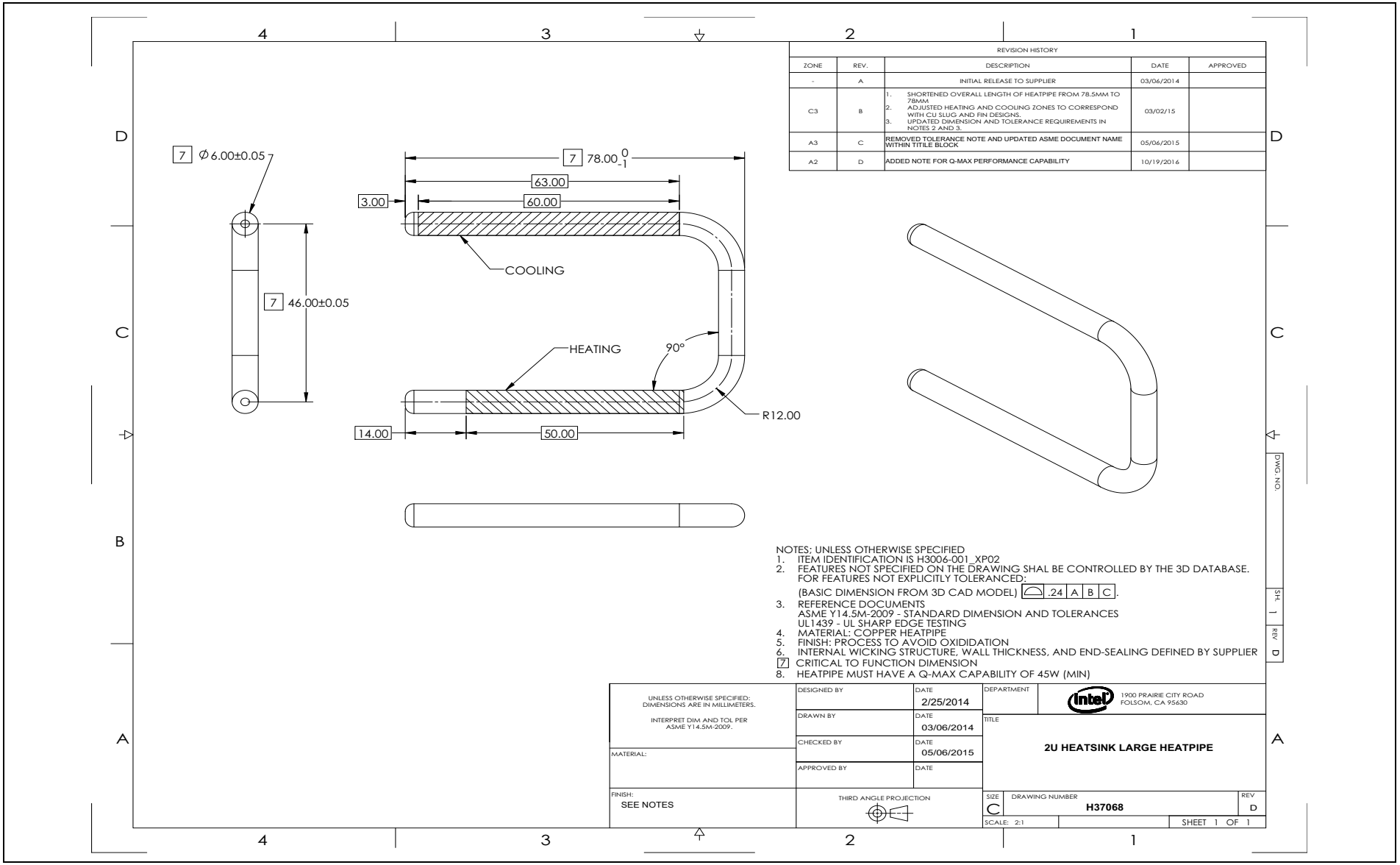


Figure E-4. 2U Heatsink Copper Slug

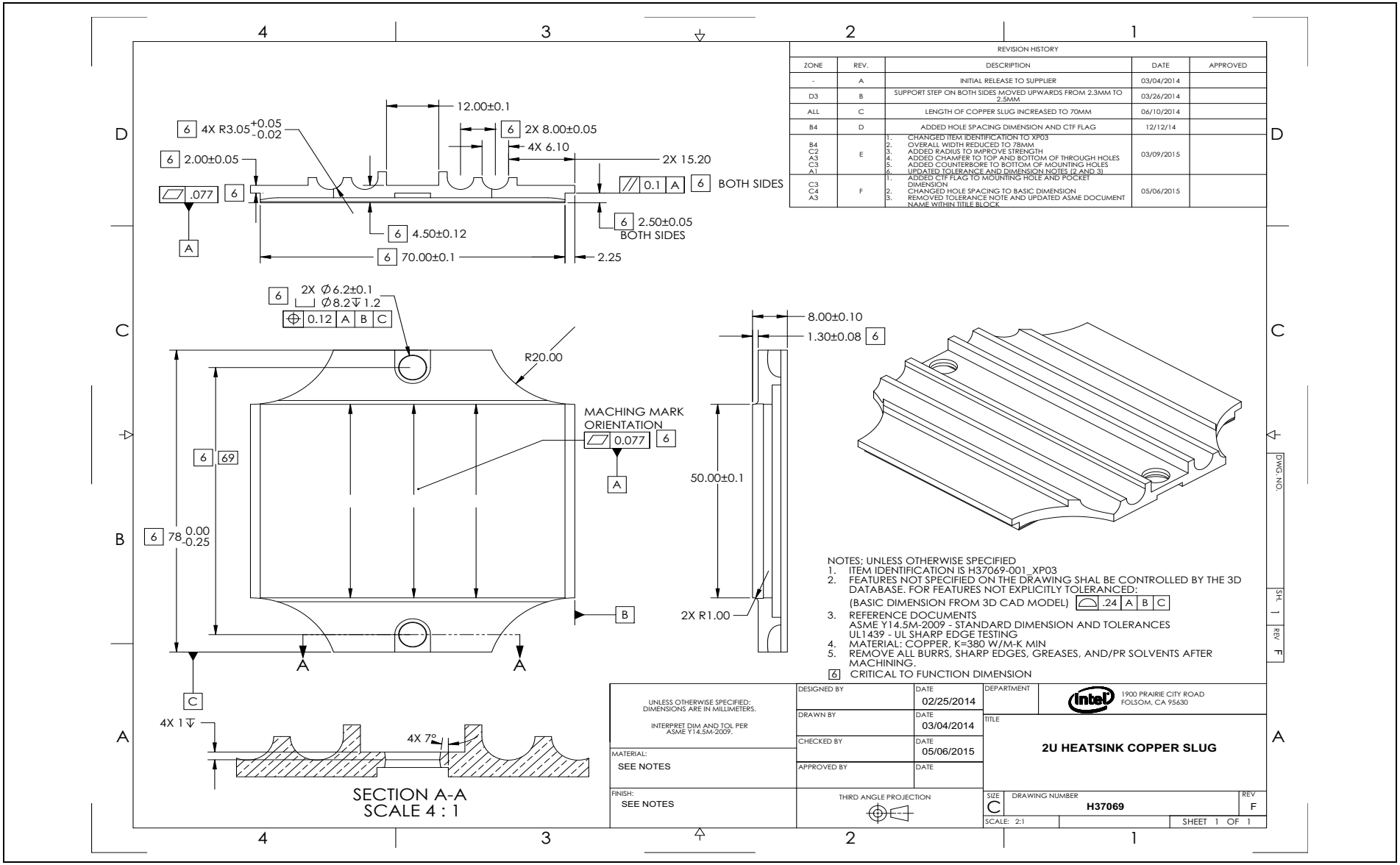


Figure E-5. 2U Heatsink Aluminum Base

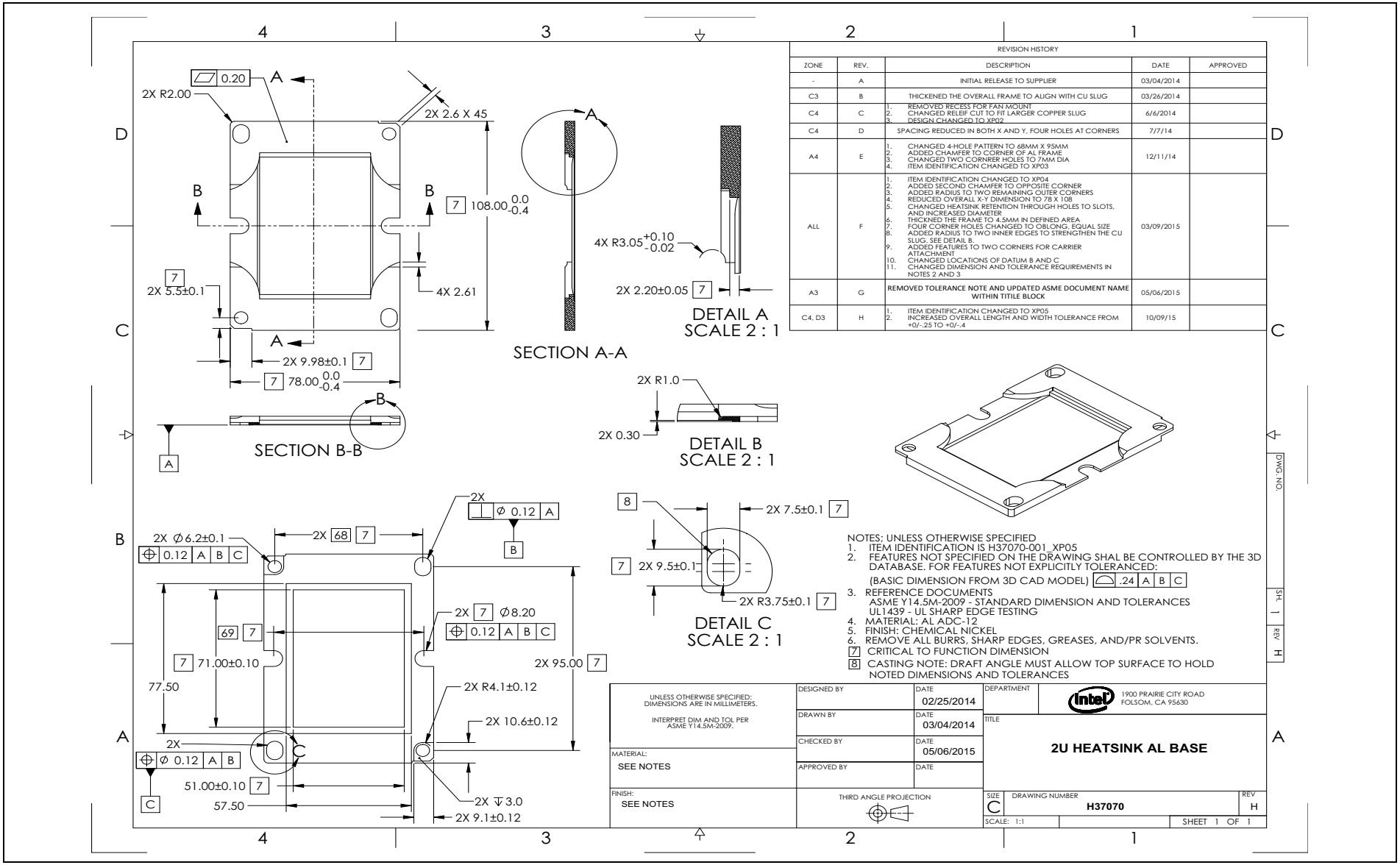


Figure E-6. 2U Heatsink Fin Assembly

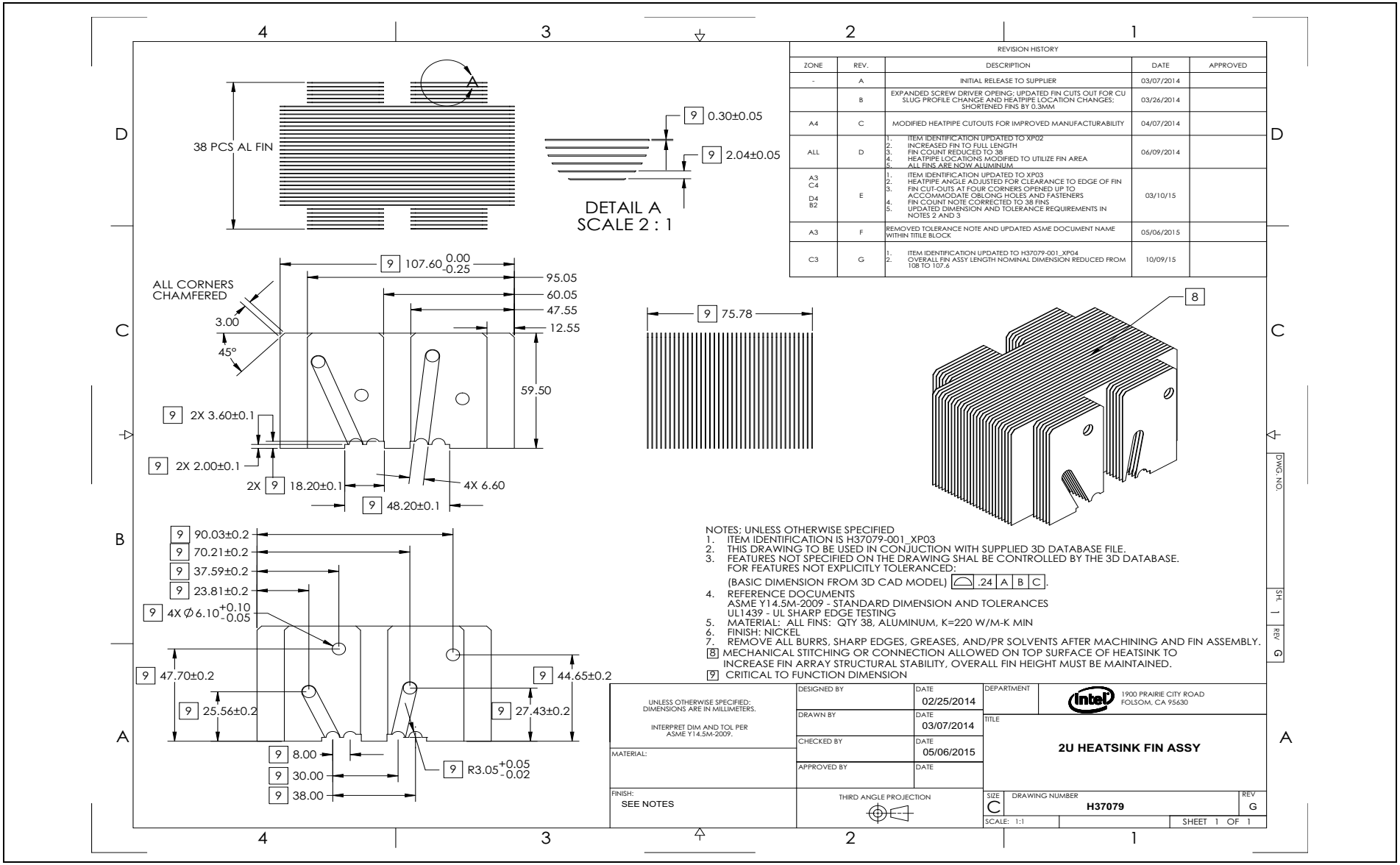


Figure E-7. Delrin Heatsink Washer

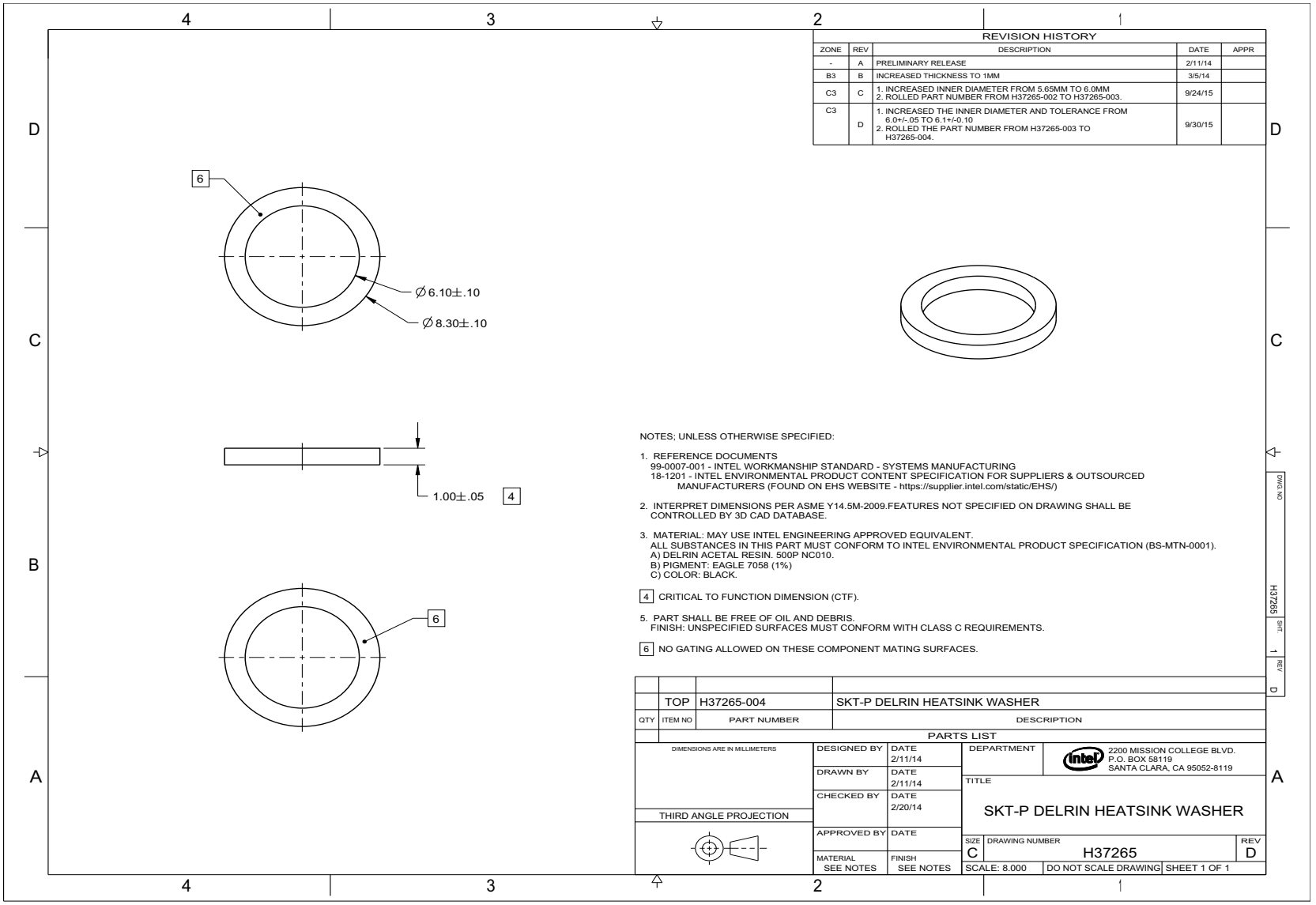


Figure E-8. TIM PCM45F

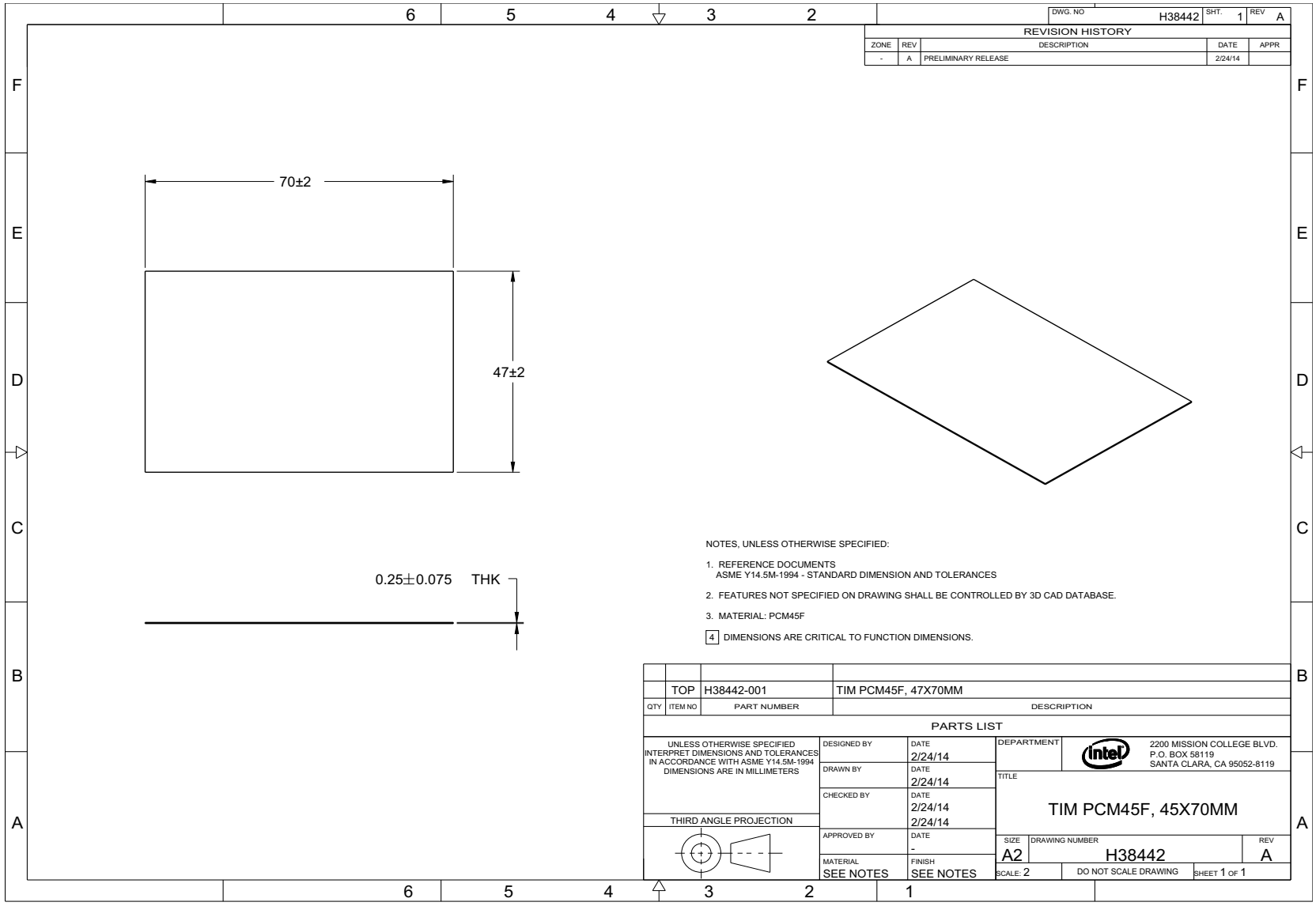


Figure E-9. 1U Heatsink Assembly (Sheet 1 of 2)

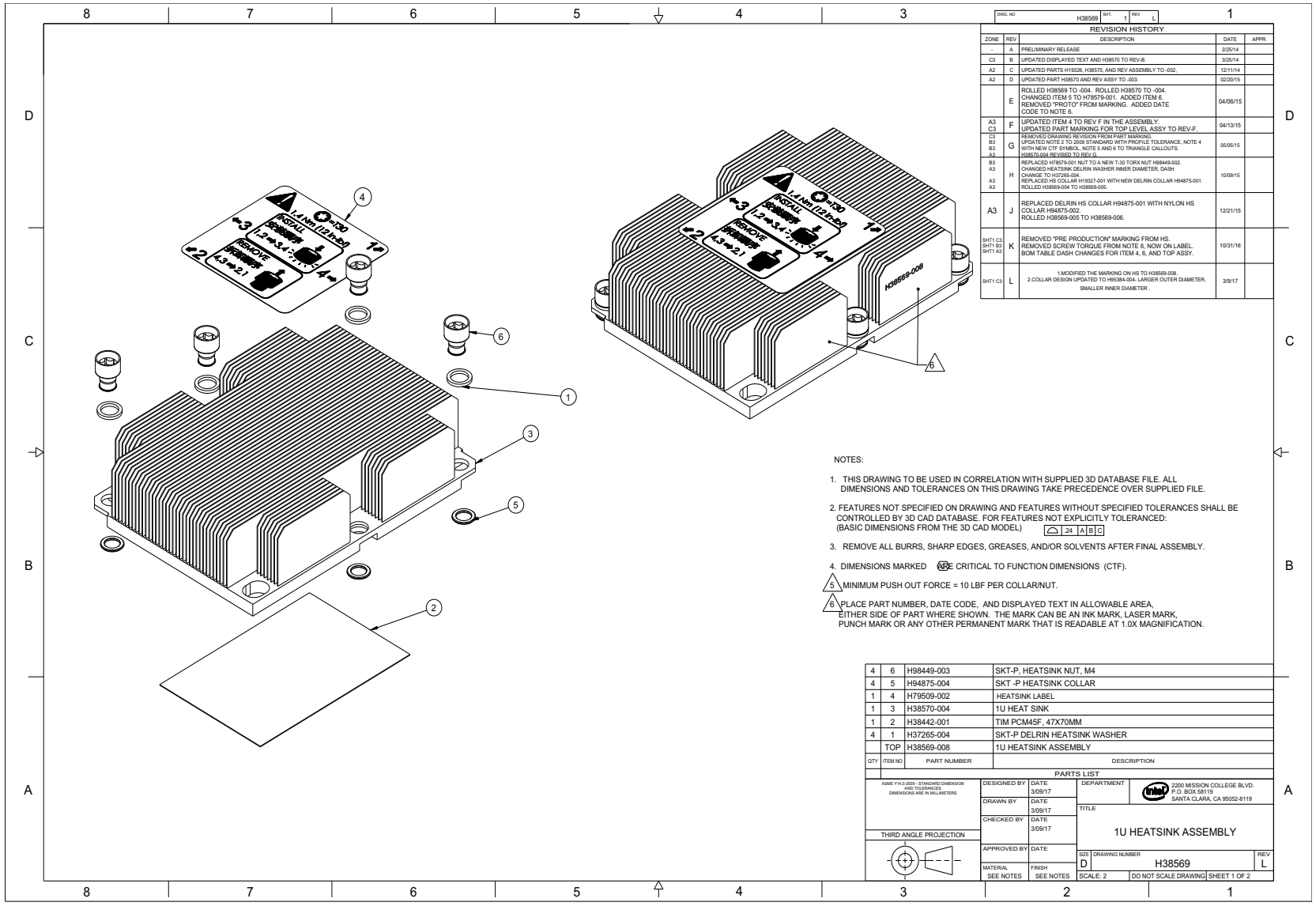


Figure E-9. 1U Heatsink Assembly (Sheet 2 of 2)

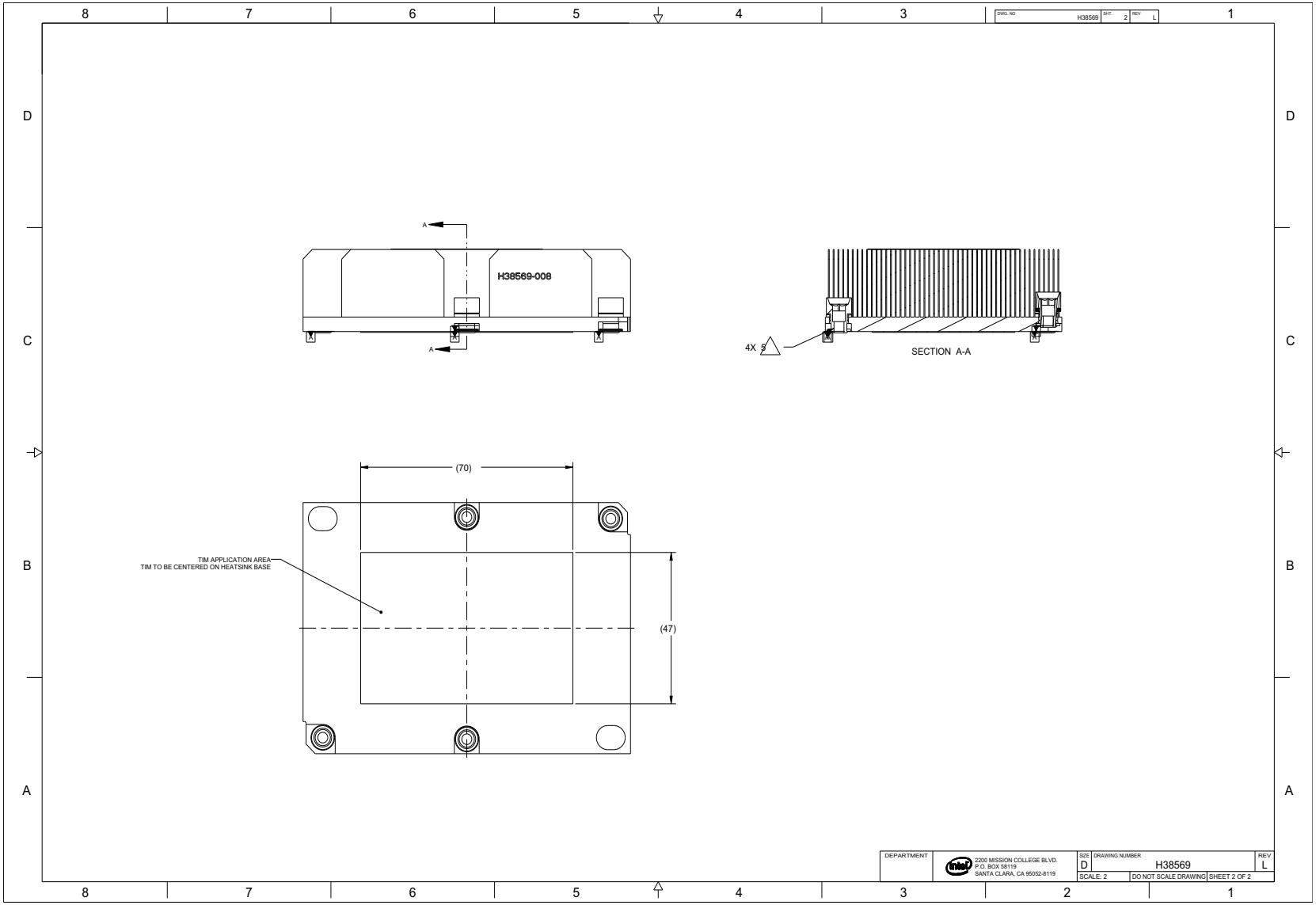


Figure E-10. 1U Heatsink (Sheet 1 of 2)

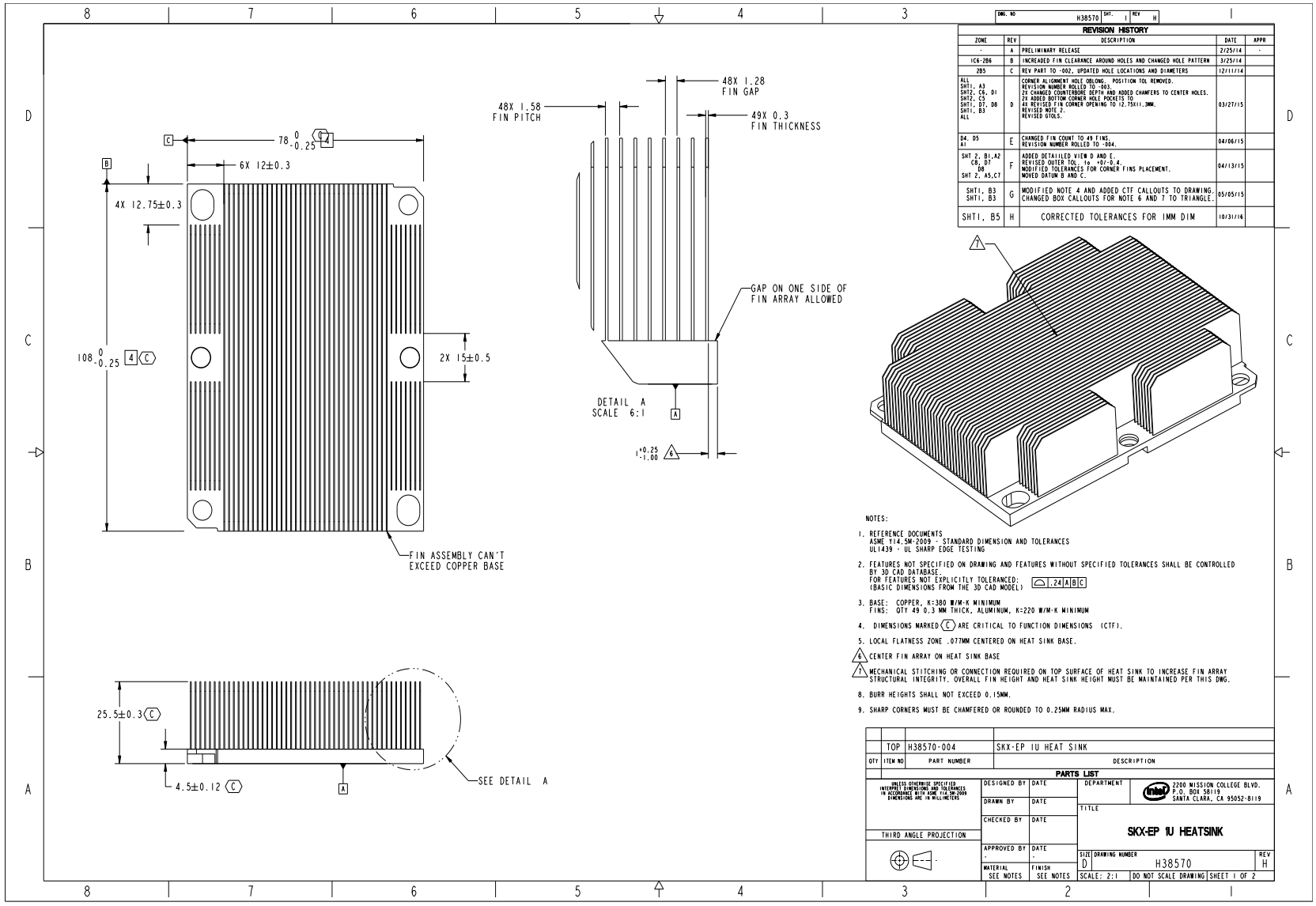


Figure E-10. 1U Heatsink (Sheet 2 of 2)

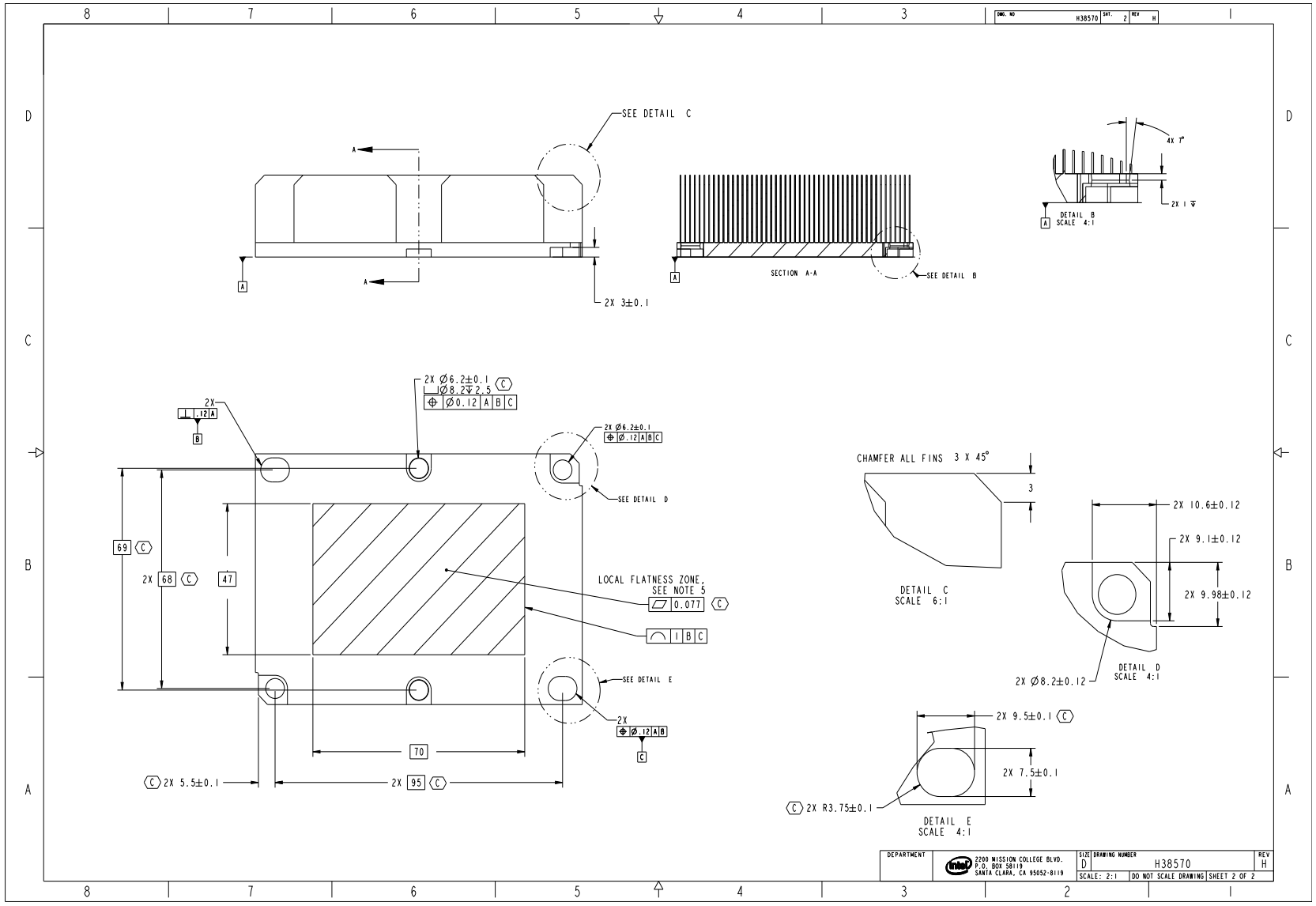


Figure E-11. 1U Extruded Heatsink Assembly (Sheet 1 of 2)

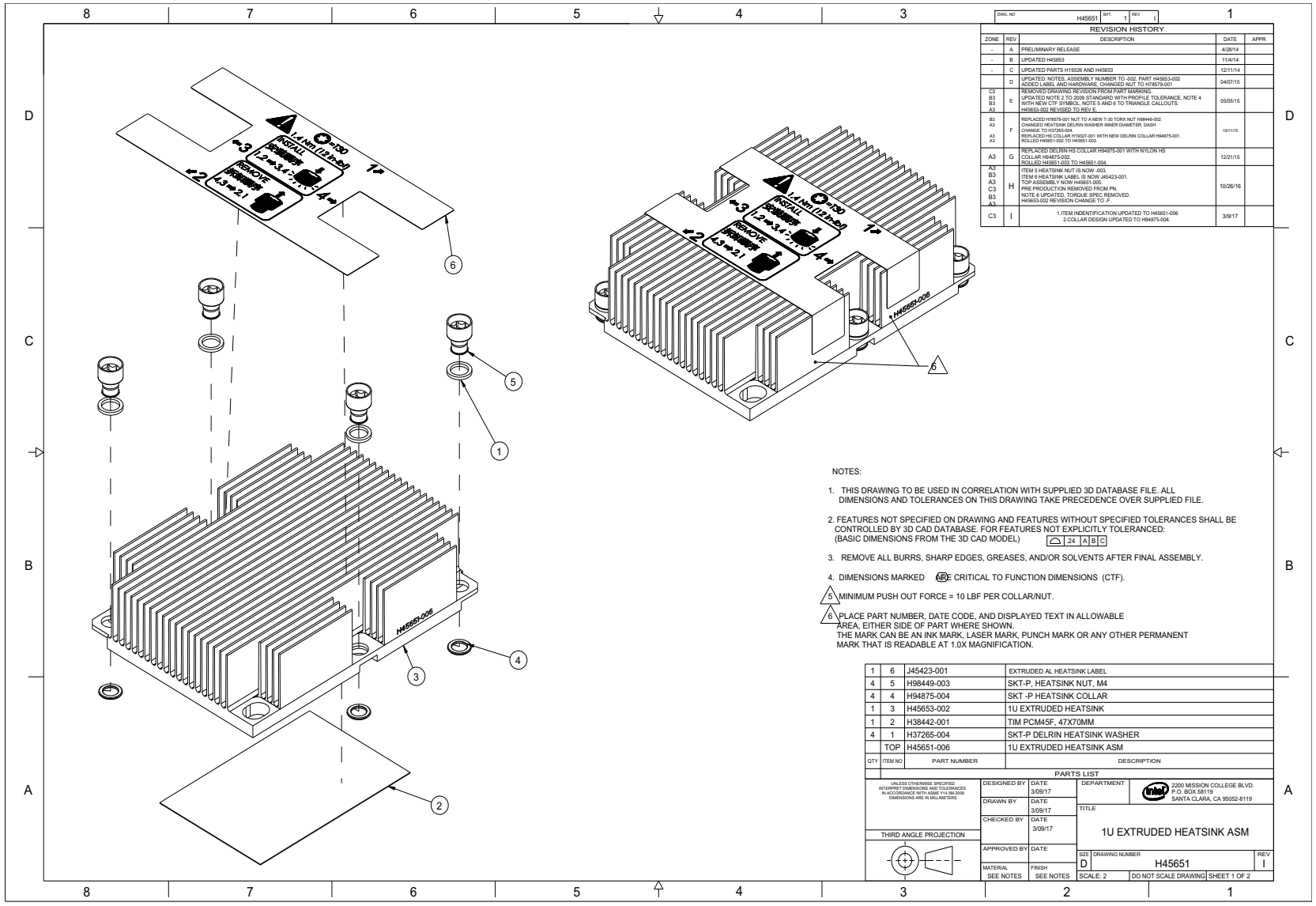


Figure E-11. 1U Extruded Heatsink Assembly (Sheet 2 of 2)

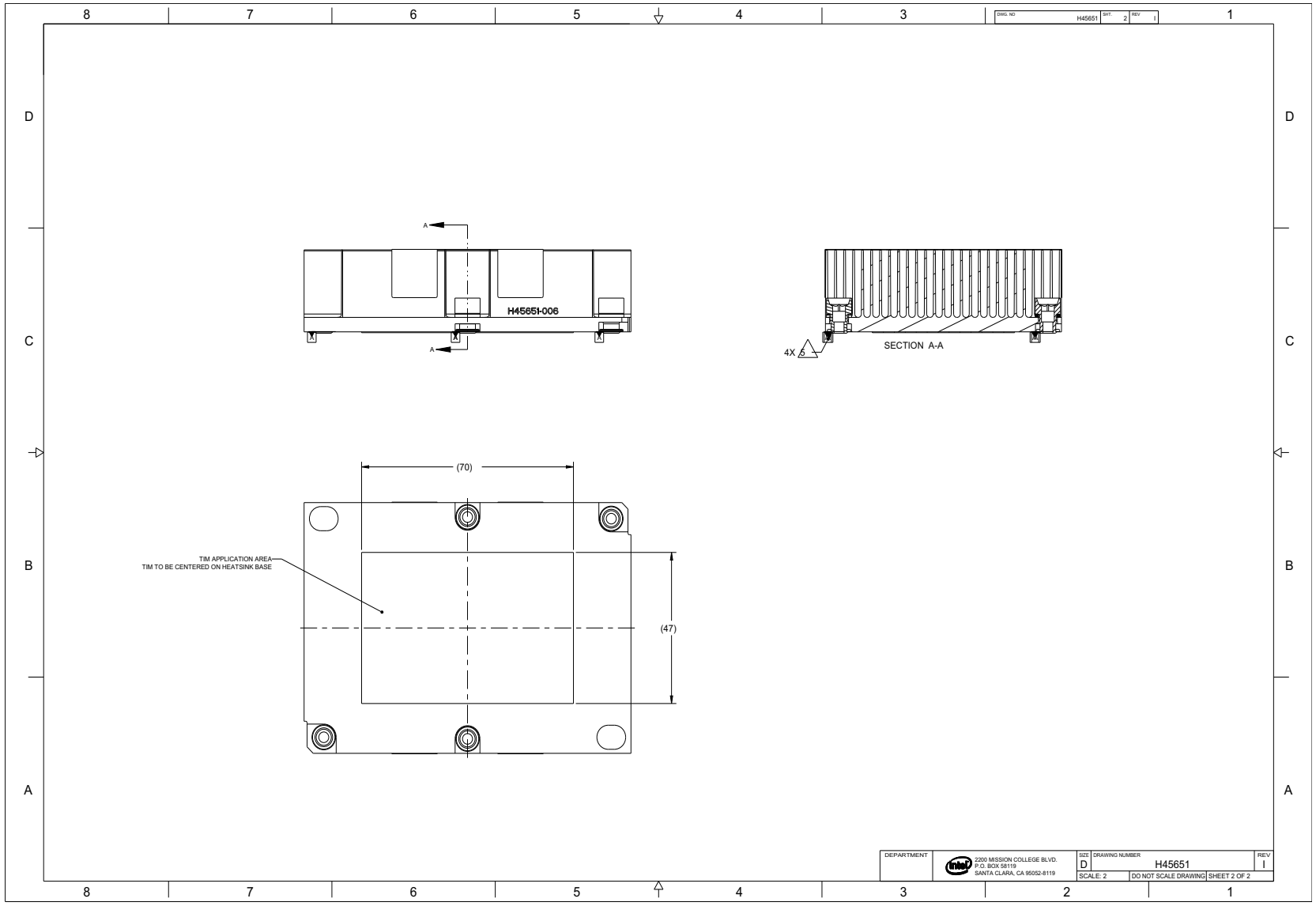


Figure E-12. 1U Extruded Heatsink (Sheet 1 of 2)

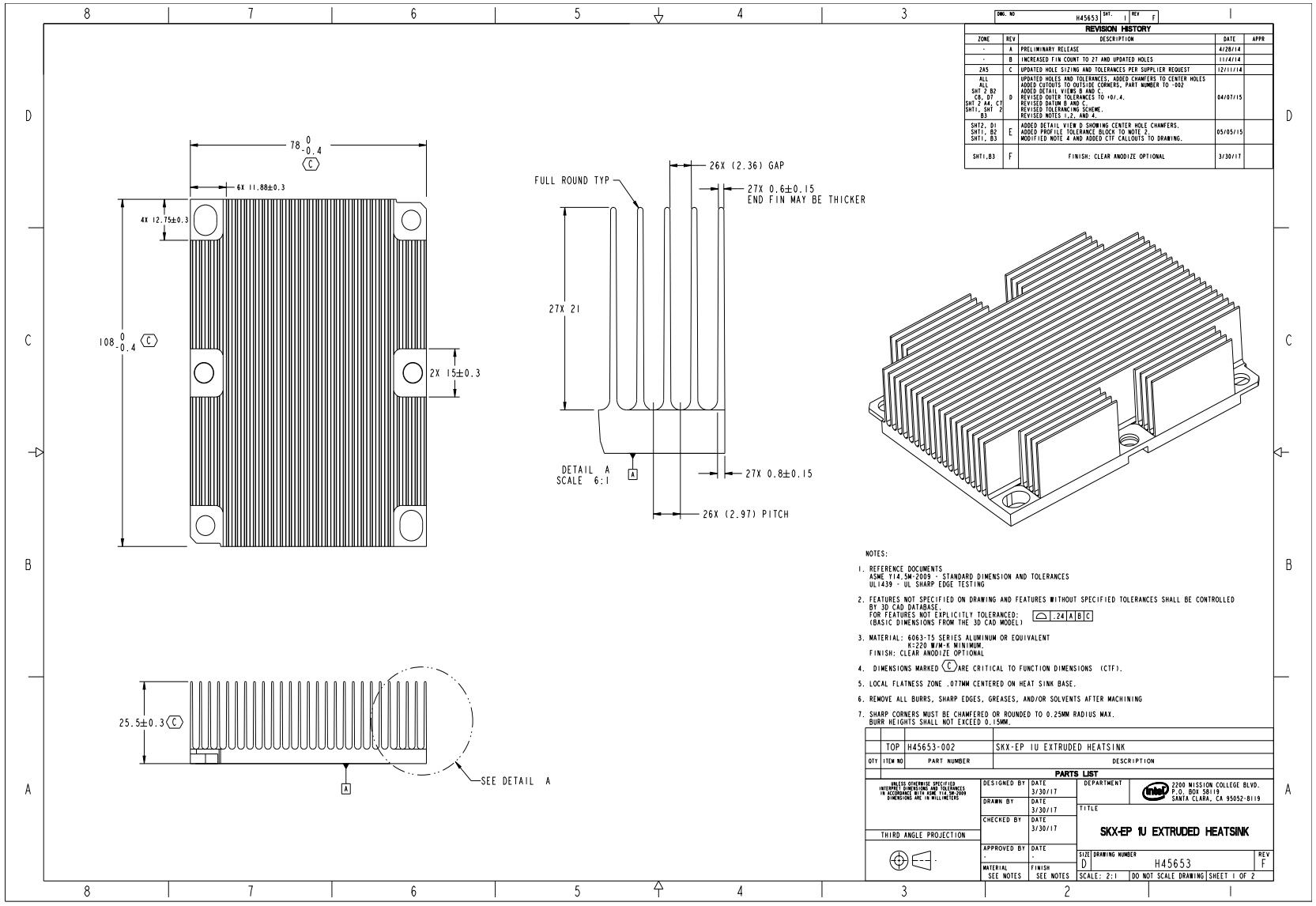


Figure E-12. 1U Extruded Heatsink (Sheet 2 of 2)

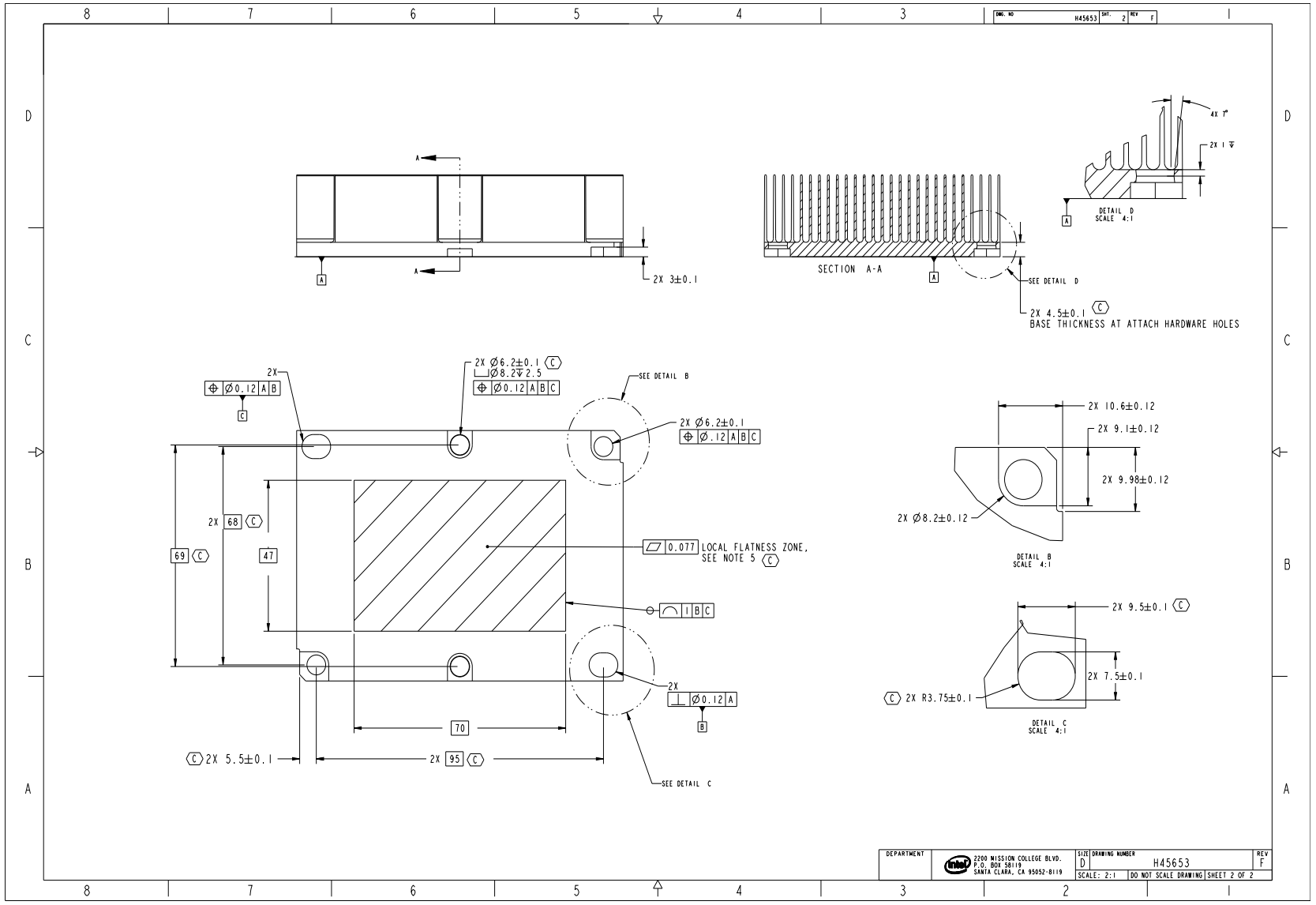


Figure E-13. Heatsink Label

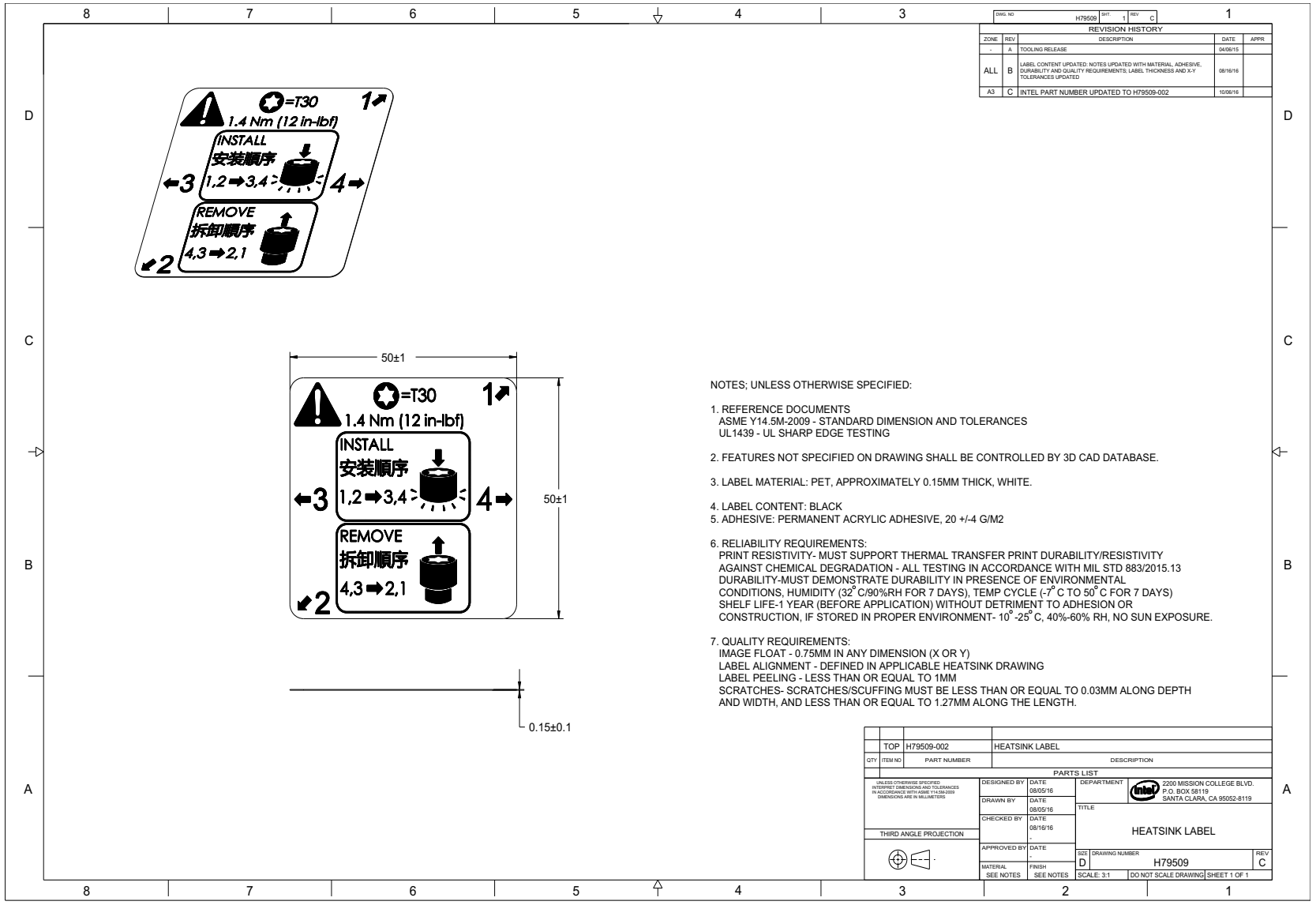


Figure E-14. Heatsink Collar

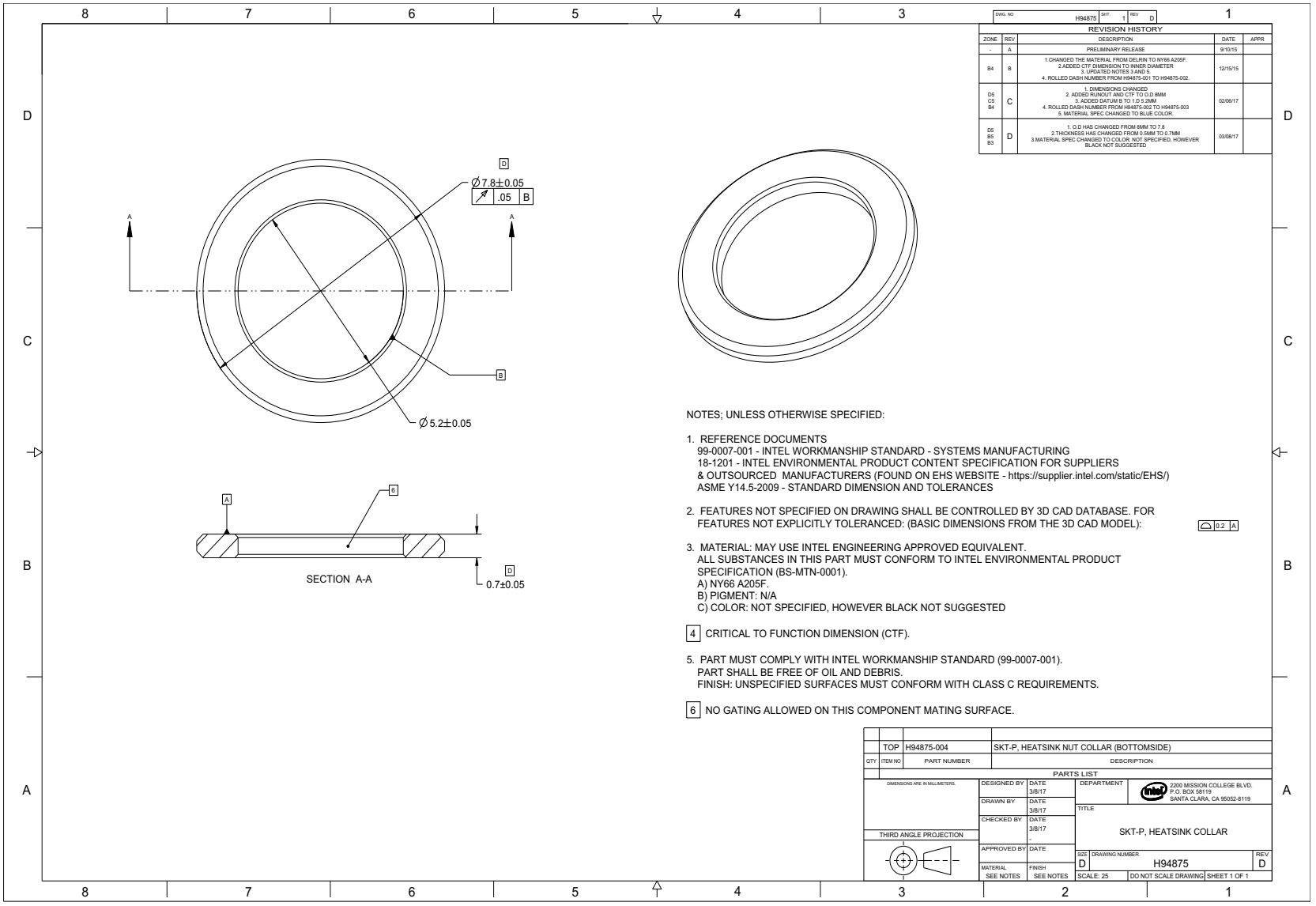


Figure E-15. Heatsink Nut (Sheet 1 of 2)

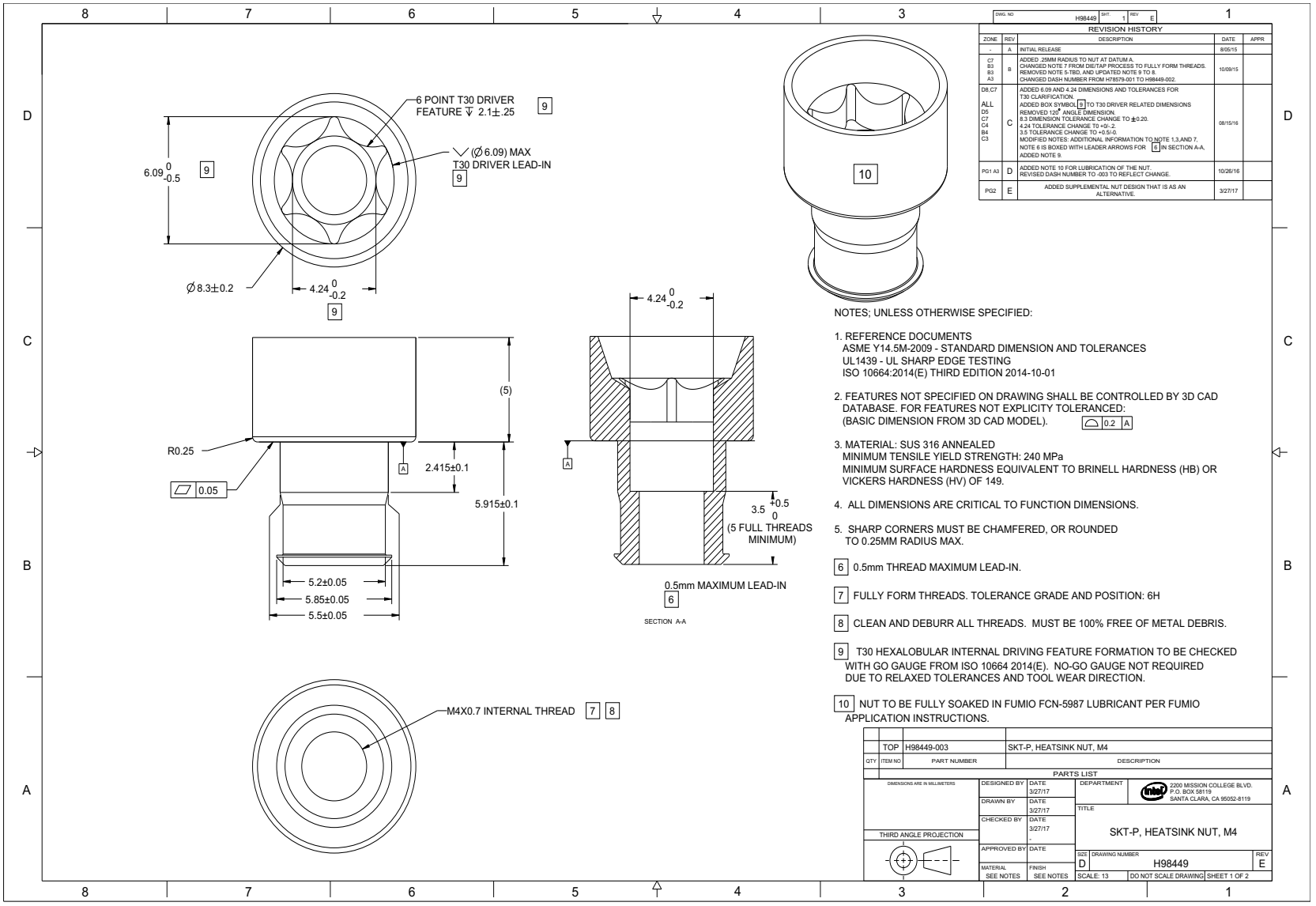


Figure E-15. Heatsink Nut (Sheet 2 of 2)

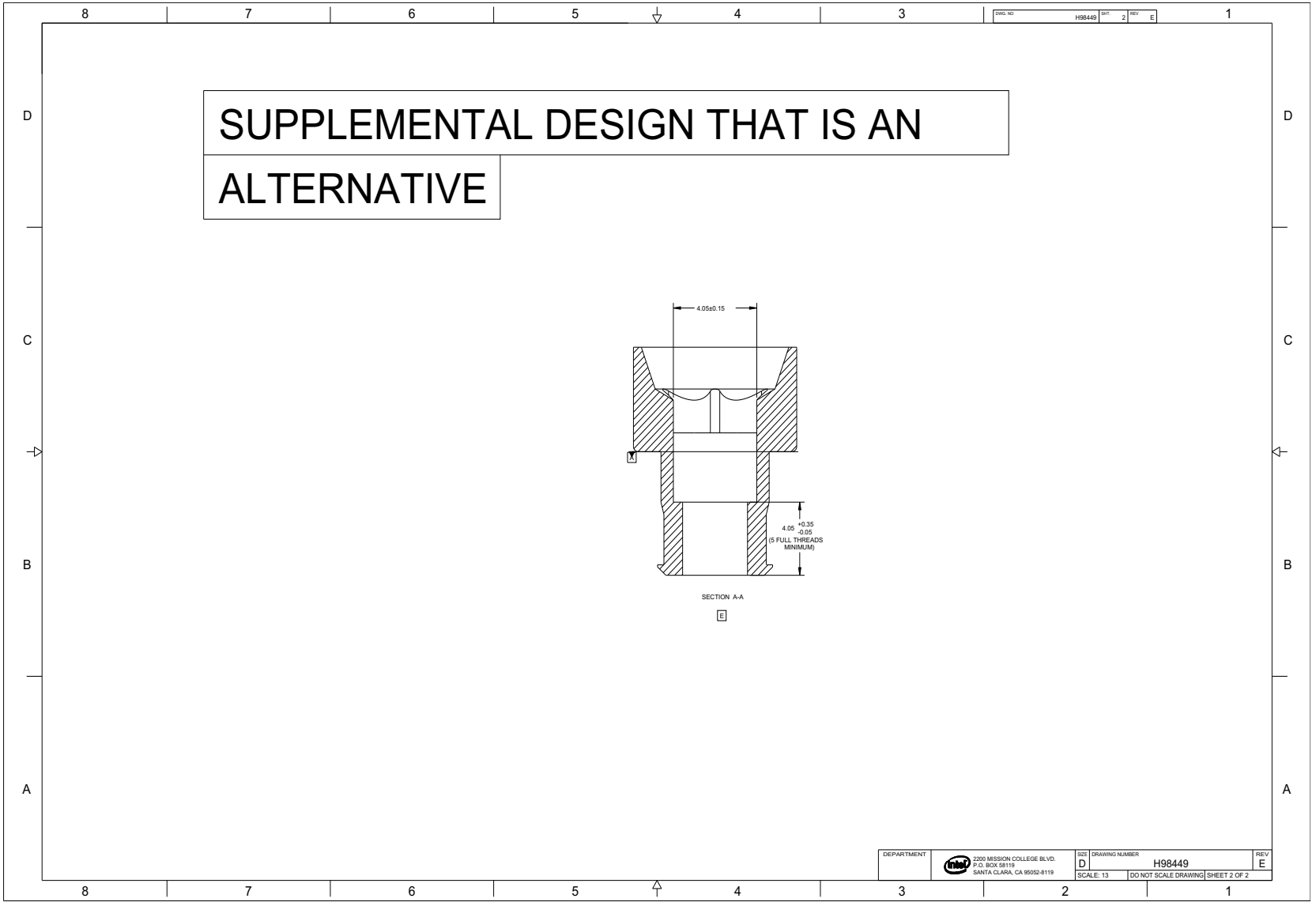
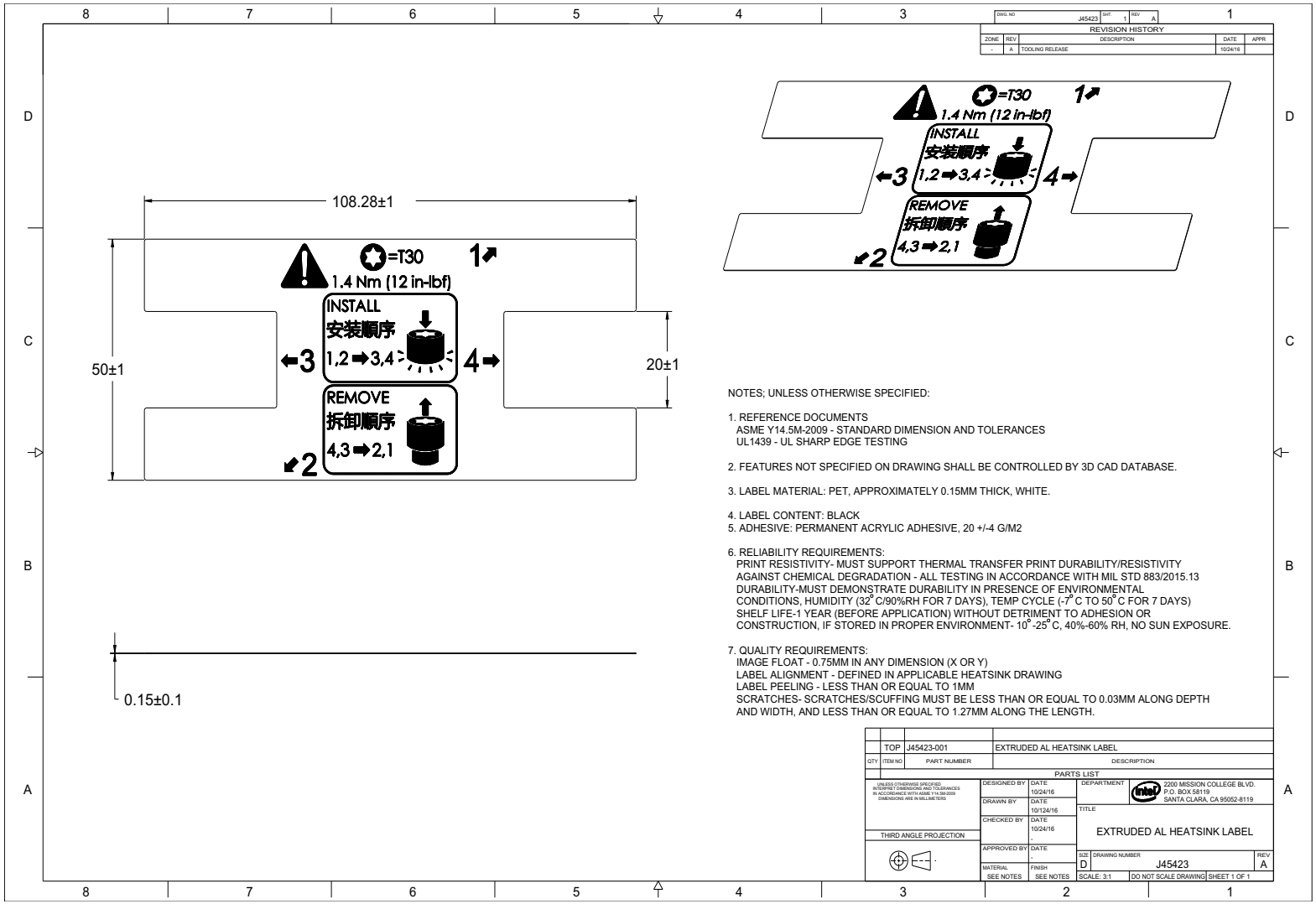


Figure E-16. Extruded Aluminum Heatsink Label



§

F Mechanical Keep-Out Zones (KOZs) Drawings

F.1 Main Board Mechanical KOZs

Processor Heatsink Module (PHM) keep-out zones are included in this chapter. Table F-1 lists the mechanical drawings included in this chapter.

Table F-1. Mechanical Keep-Out Zone Drawing List

Description	Figure
KOZ: PHM 6 Holes	Figure F-1
KOZ: PHM Narrow Backplate	Figure F-2
KOZ: PHM Narrow Master (Sheet 1 of 6)	Figure F-3
KOZ: PHM 7 Holes	Figure F-9

Figure F-1. KOZ: PHM 6 Holes

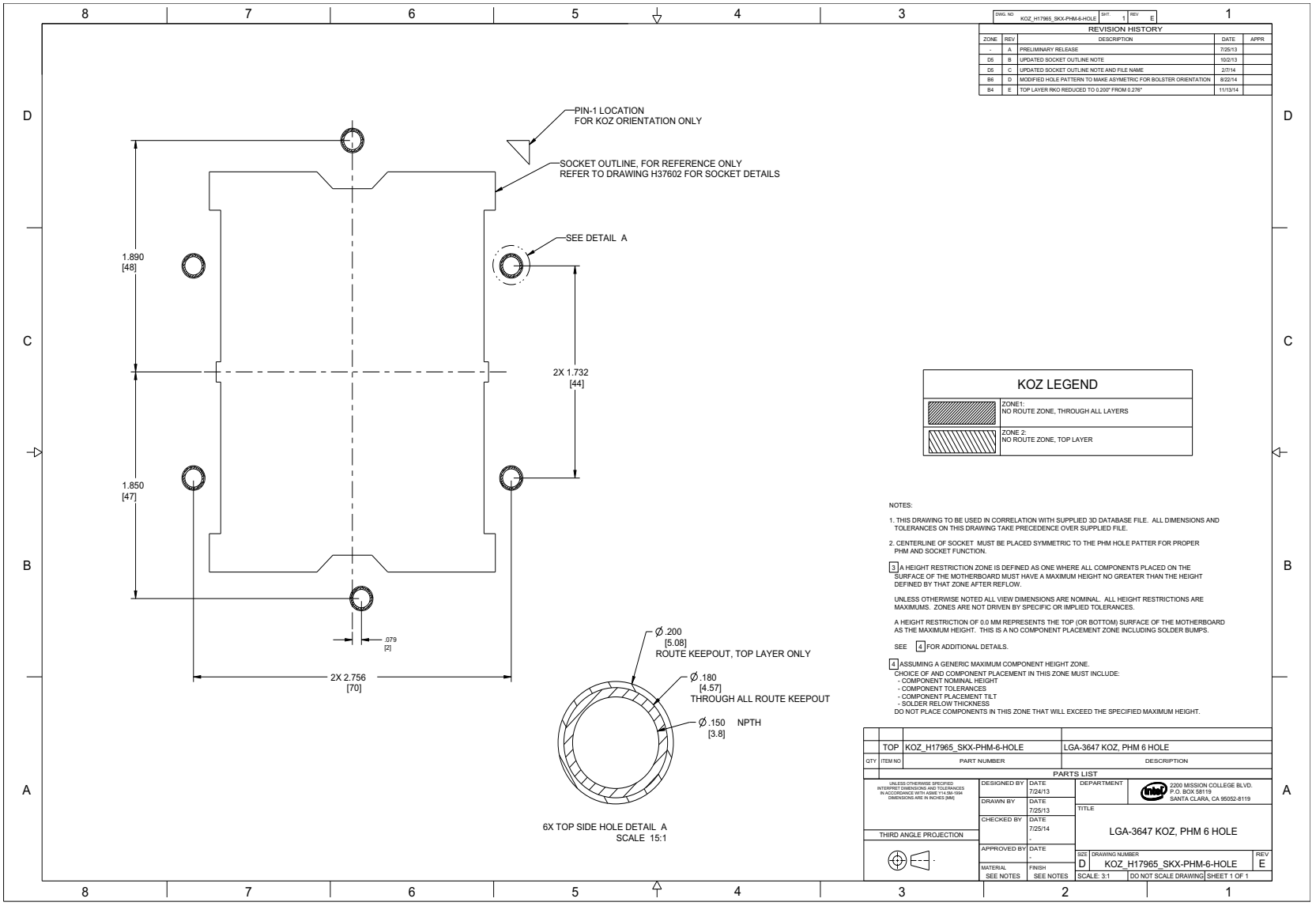


Figure F-2. KOZ: PHM Narrow Backplate

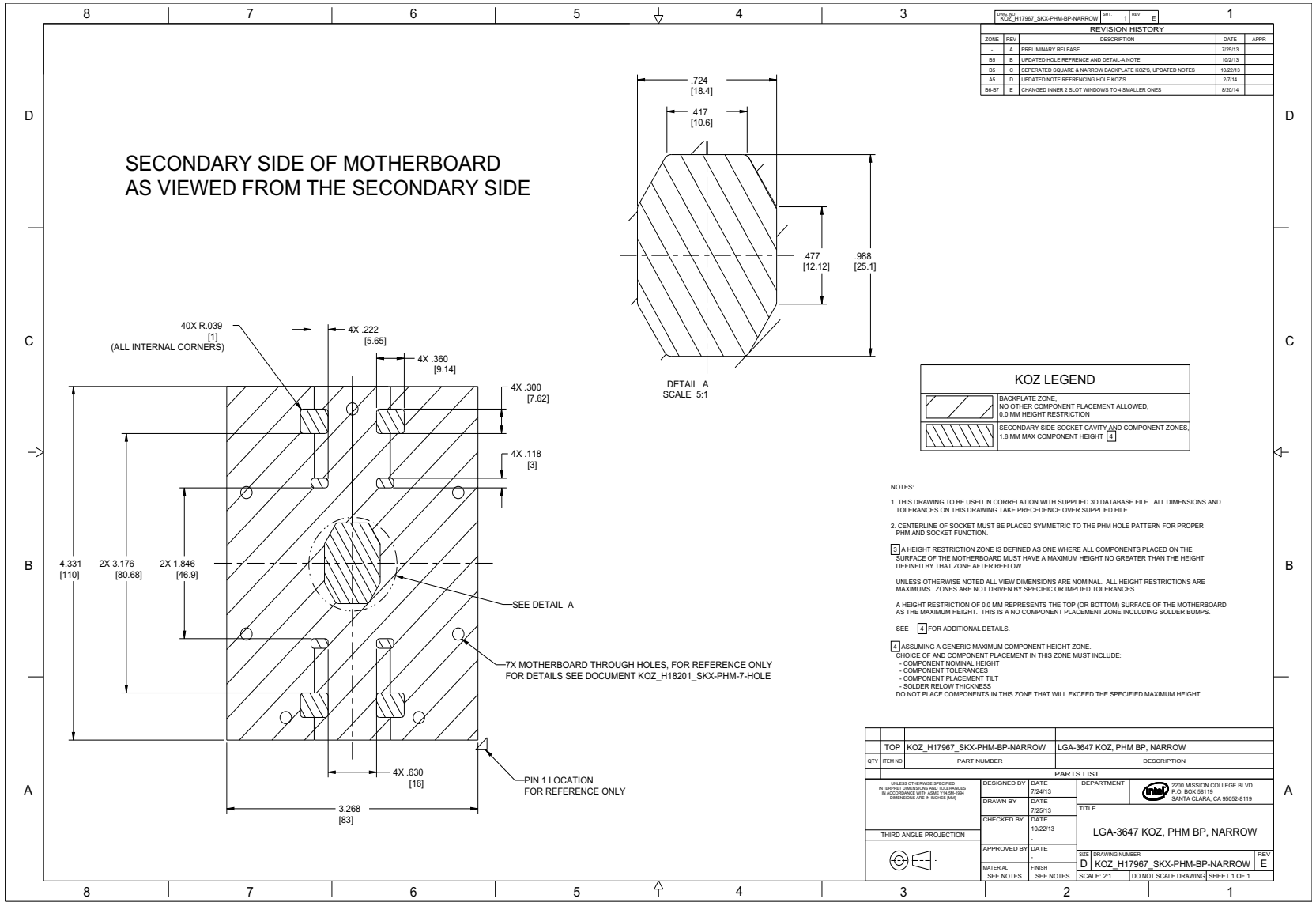


Figure F-3. KOZ: PHM Narrow Master (Sheet 1 of 6)

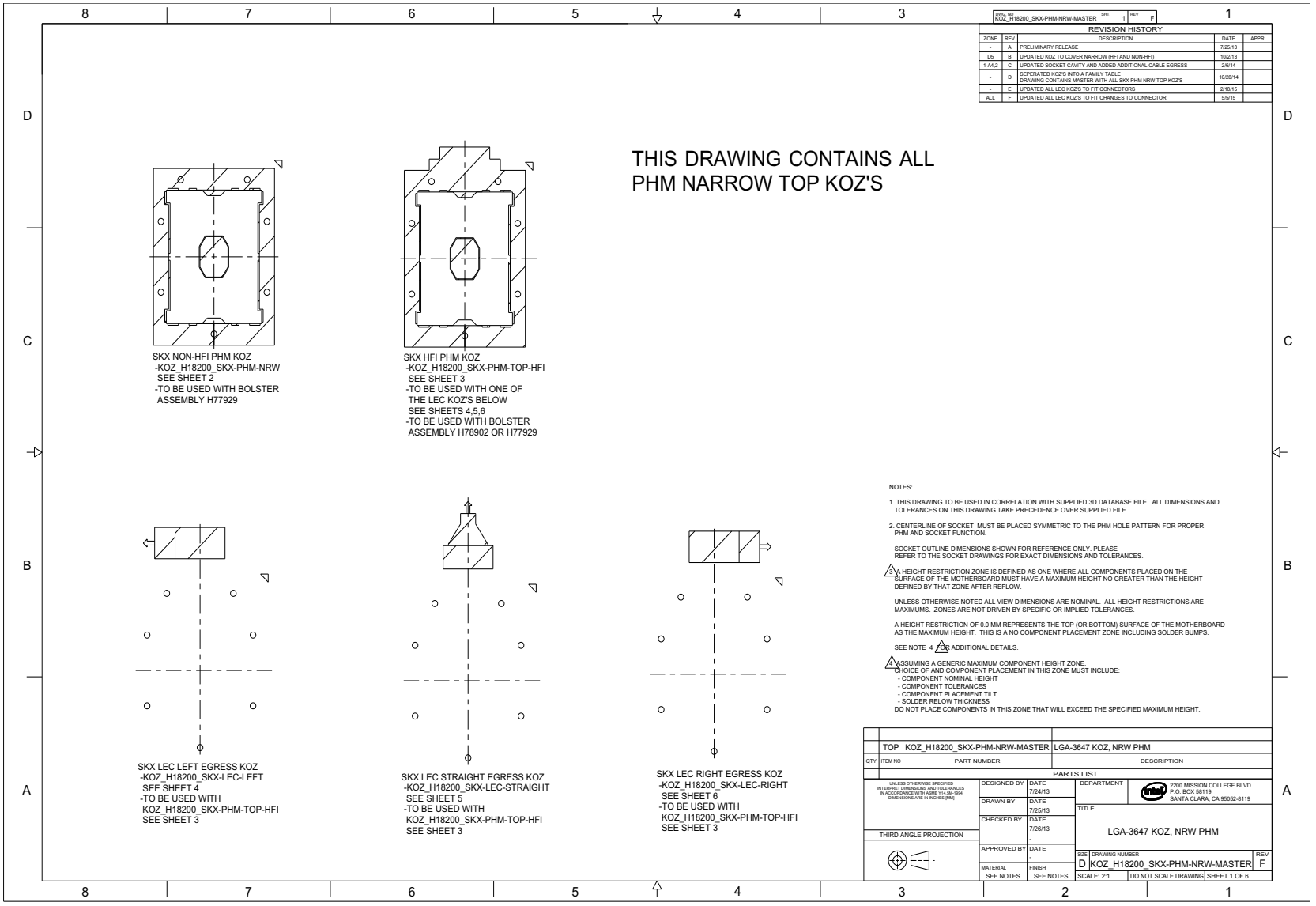


Figure F-4. KOZ: PHM Narrow Master (Sheet 2 of 6)

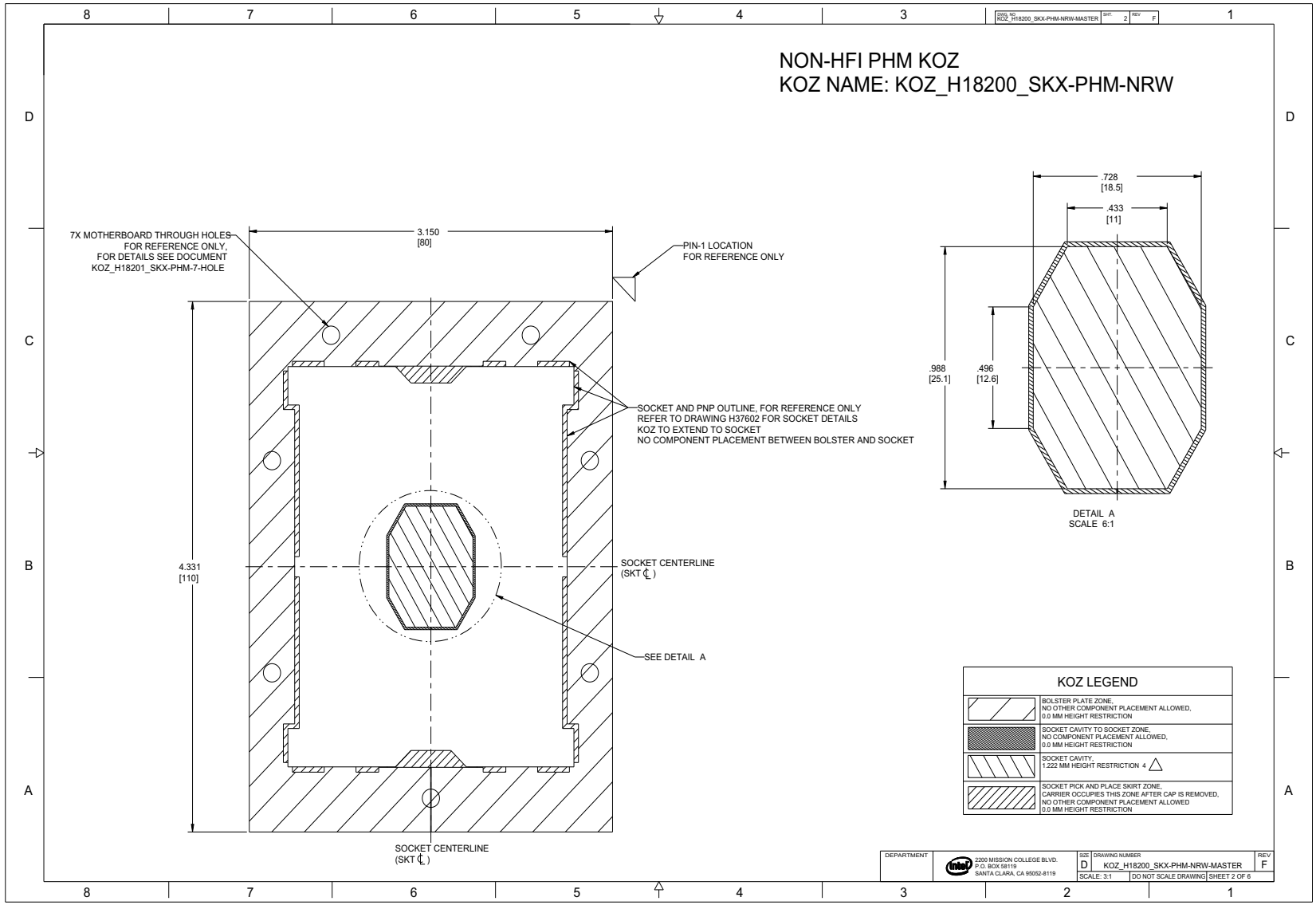


Figure F-5. KOZ: PHM Narrow Master (Sheet 3 of 6)

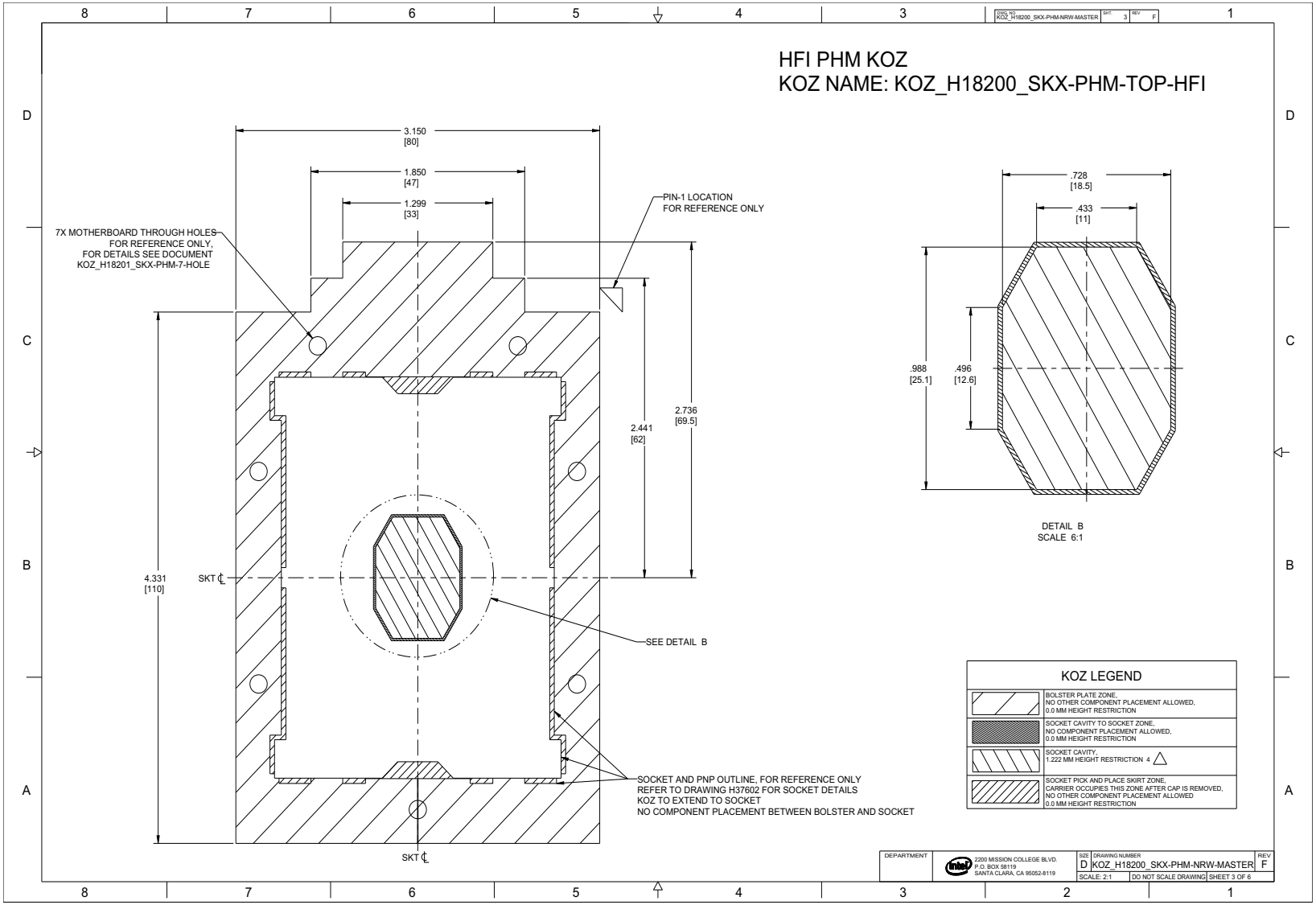


Figure F-6. KOZ: PHM Narrow Master (Sheet 4 of 6)

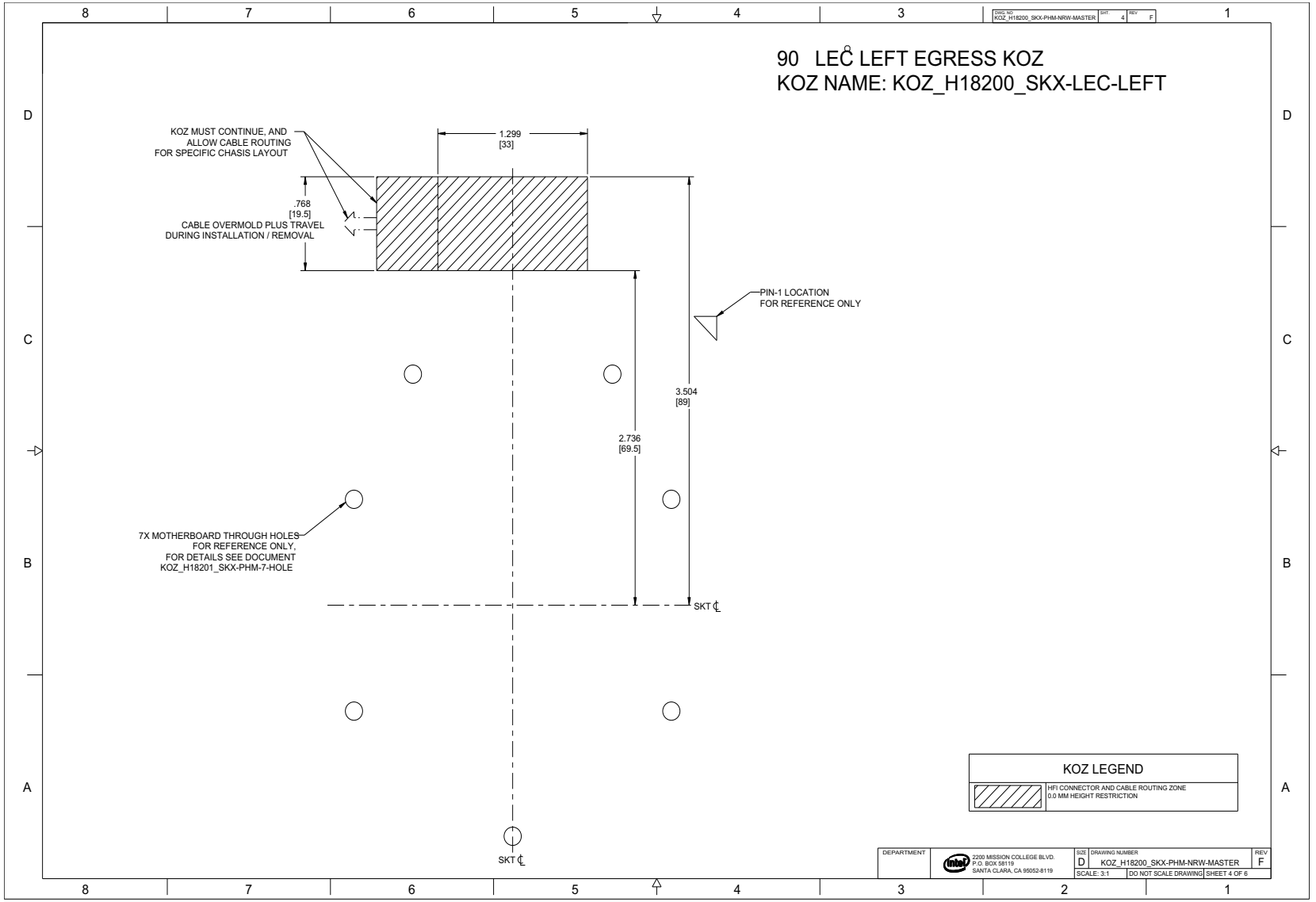


Figure F-7. KOZ: PHM Narrow Master (Sheet 5 of 6)

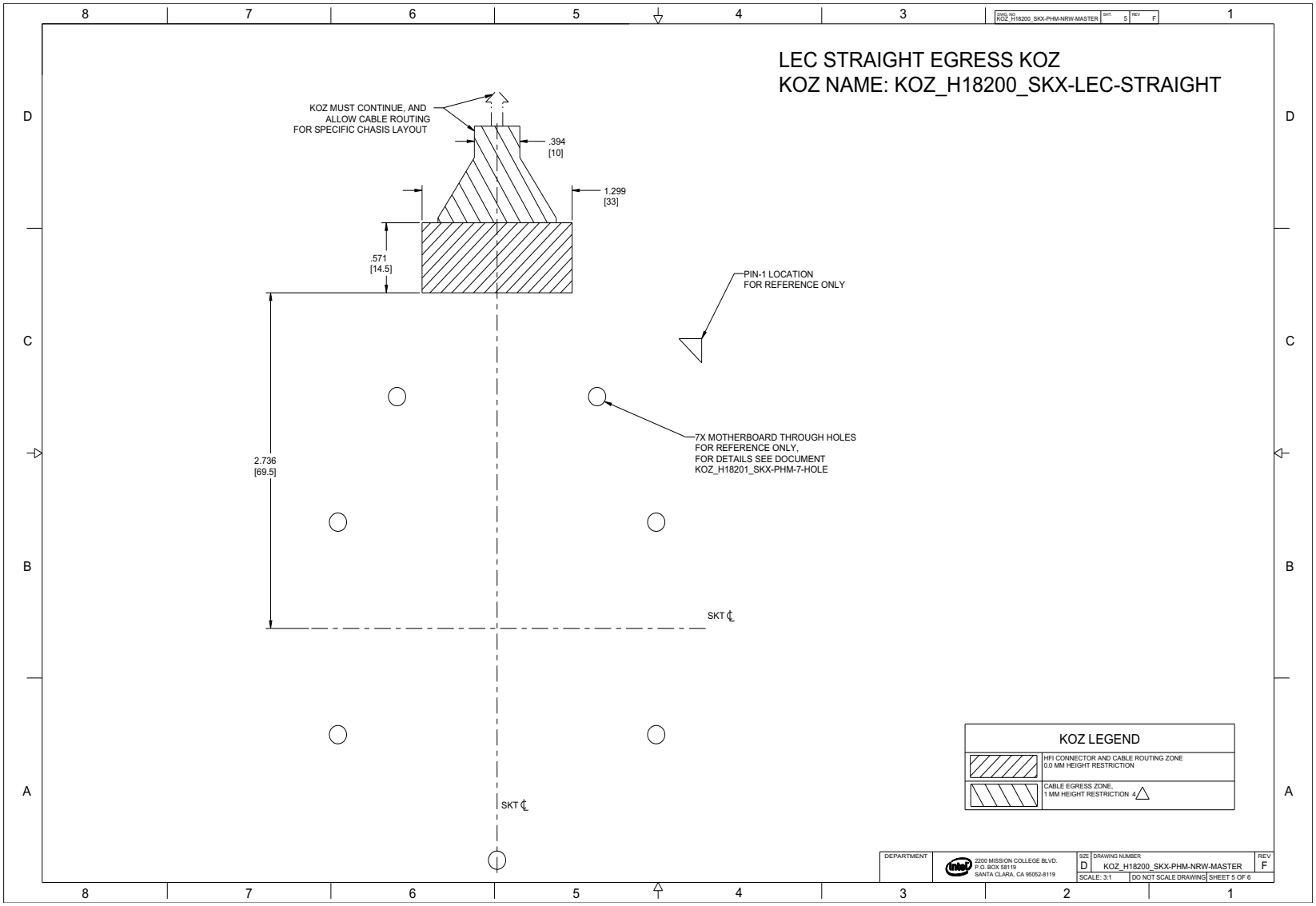


Figure F-8. KOZ: PHM Narrow Master (Sheet 6 of 6)

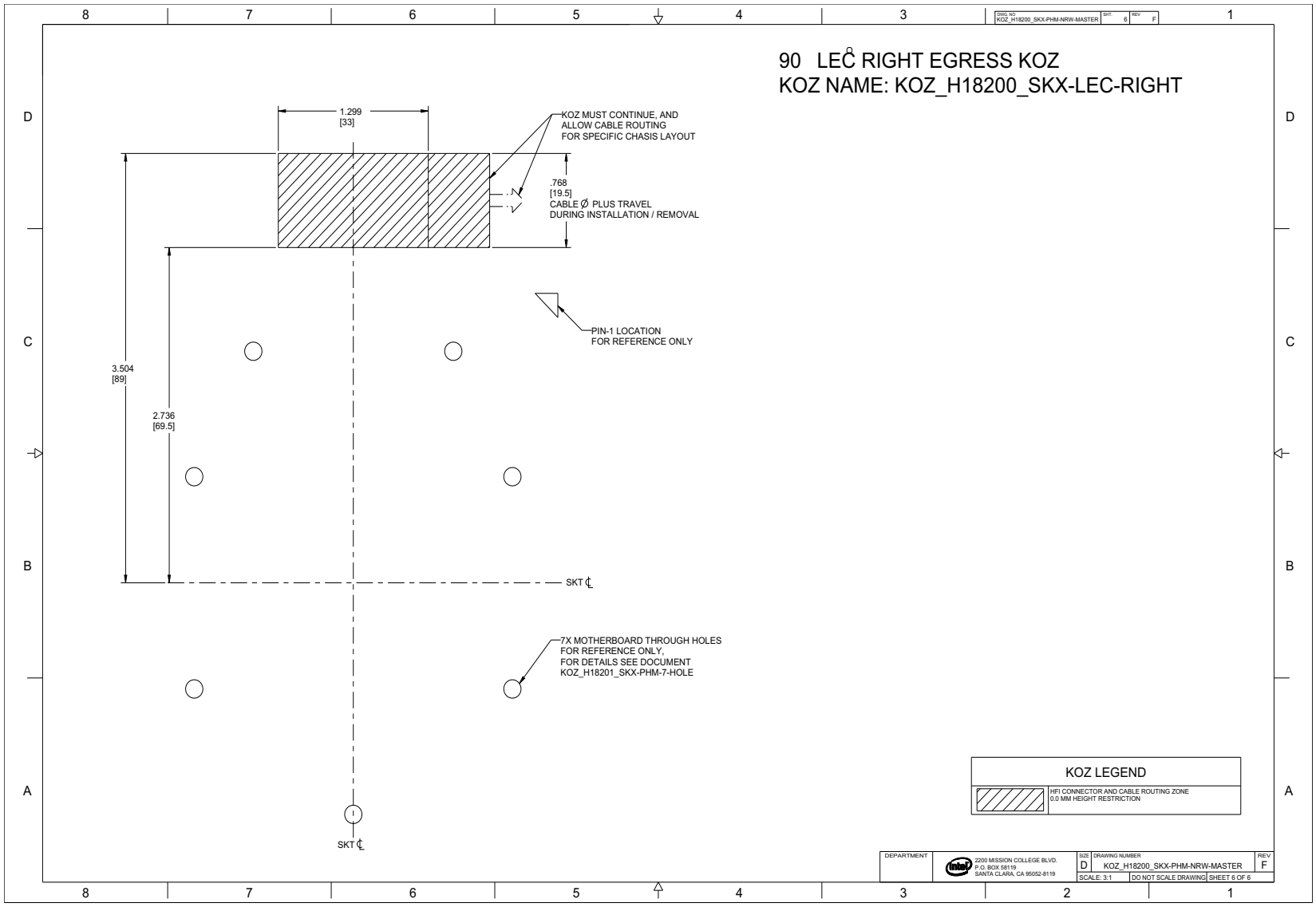
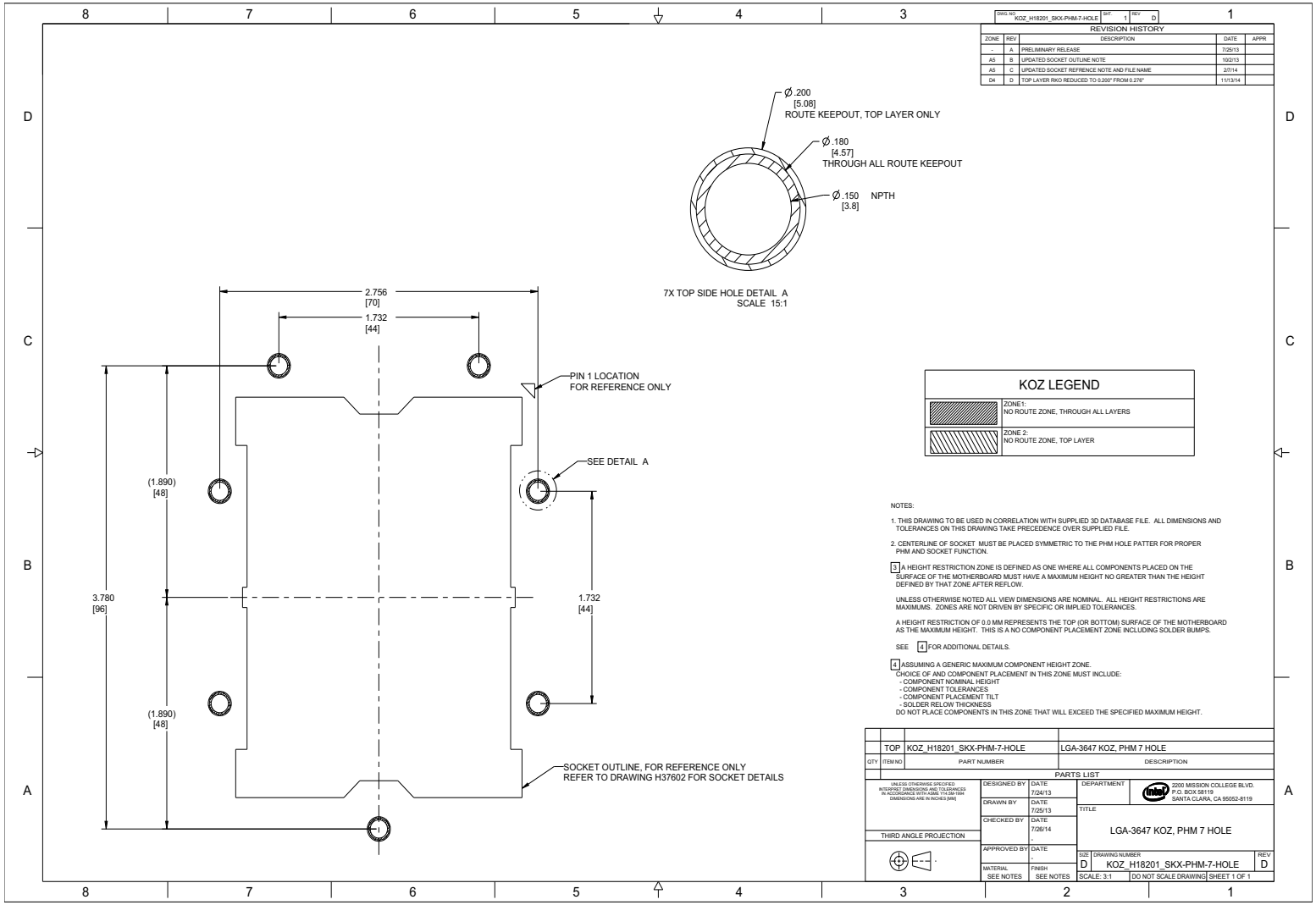


Figure F-9. KOZ: PHM 7 Holes



§

G Board Flexure Initiative

Figure G-1. LGA3647 Socket BFI (Sheet 1 of 2)

BFI STRAIN GUIDANCE SHEET
REV 0.0

Component	LGA 3647 (Socket P)
Socket Size	62 x 82 mm
Pitch	0.9906 mm Pitch
Pin Count	3647

Scope: The strain values provided in this document apply only to transient bend conditions seen in board manufacturing assembly environment with no PHM and does not apply once PHM is installed.

Gage Location: Strain gages must be placed at 4 locations on the board at 12.0 mm from corner solder joint, measured along the diagonal, with e1 and e3 parallel to the edges. Alternatively, the gage can be located with reference to socket housing. Please refer to figures 2 through 5 for locating strain gage on all four corners. Accurate positioning of the strain gages is necessary to compare strain data to Intel's BFI strain guidance. Strain gage location accuracy should be +/-0.5 mm and +/- 5°.

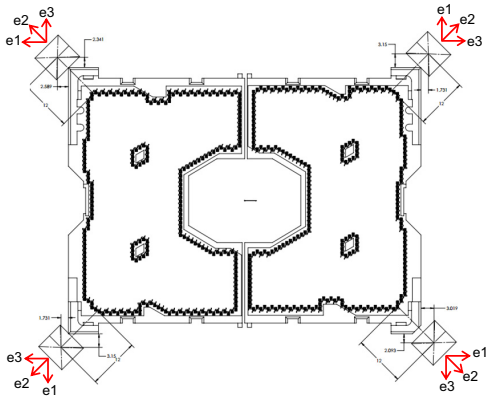


Figure 1 Gage placement at all four corners

Intel Confidential
May 2015

Figure G-2. LGA3647 Socket BFI (Sheet 2 of 2)

BFI STRAIN GUIDANCE SHEET
REV 0.0

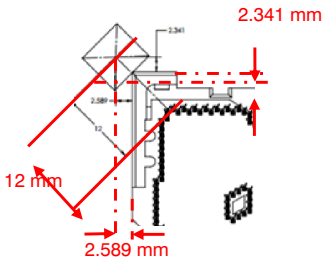


Figure 2 Gage placement at pin FF86 corner

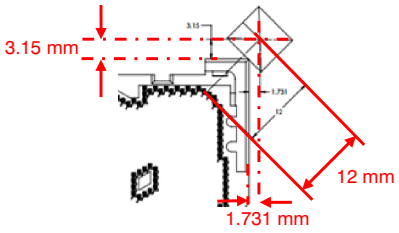


Figure 3 Gage placement at pin FF1 corner

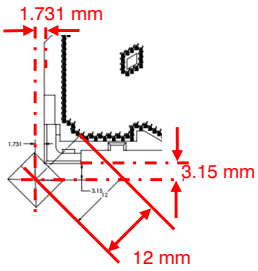


Figure 4 Gage placement at pin A86 corner

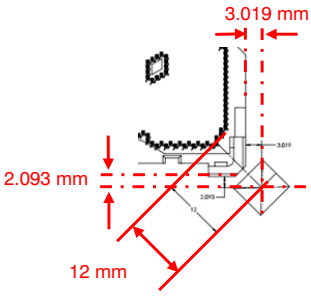


Figure 5 Gage placement at pin A1 corner

Test Requirements: The Maximum Diagonal Strain for all (4) corners, is not to exceed the values listed in the table. The Diagonal Strain formula is defined as:

Max Diagonal Strain= MAX (|e2| , |e1+e3-e2|)

Where e1, e2, & e3, are the raw strain readings from the three gages in the rosette, and the numbers inside the vertical bars are absolute values.

	0.093" Board
Lead Free	450ue Diag

Data parameters:

1. Minimum sample rate is 500Hz, recommended maximum sample rate is 2000 Hz.
2. All gages must be sampled simultaneously. (Minimum of 3 channels)
3. The output data must record, Time (t), e1, e2, and e3 for all gages. The file can be a .TXT, or .XLS format.

Reference Documents

Intel Board Flexure MAS rev 5.0 (or later) "Manufacturing with Intel Components: Strain measurement for Circuit Board Assembly"

Module 1 Overview
Module 2 Test Board Preparation
Module 3 Assembly line measurement procedure
Module 4 Reporting Procedure
Module 5 Reducing Board Flexure in ICT
Module 6 Troubleshooting

Intel Confidential
May 2015

§